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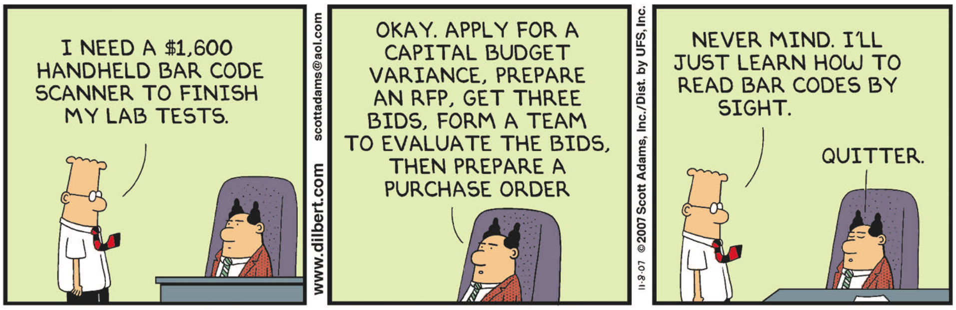

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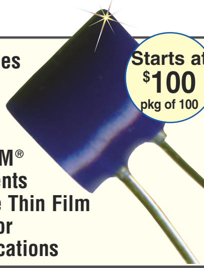

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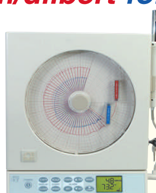

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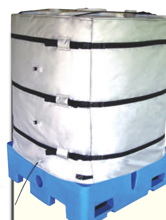

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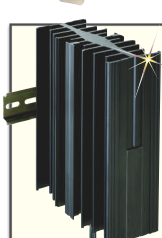

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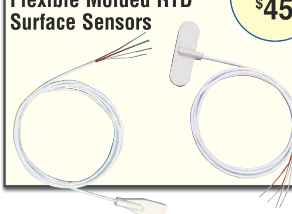

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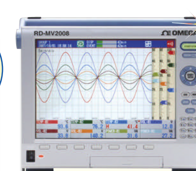

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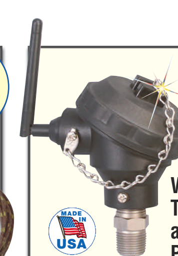

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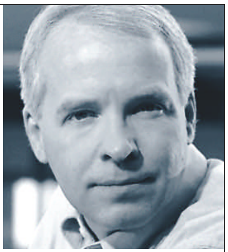

Big tester on campus

Test research is getting a helping hand through a cooperative effort of the Semiconductor Test Consortium (STC) and Auburn University. With STC support, Auburn has won a National Science Foundation grant to obtain an open-architecture semiconductor test system, which will enable much needed research into integrated-circuit test.

In an interview at the International Test Conference, Paul Roddy, a technical manager at Advantest, and Adit Singh, the James B. Davis Professor at the Department of Electrical and Computer Engineering at Auburn and chair of the IEEE Test Technology Technical Council, discussed Auburn's acquisition of the tester. Said Roddy, "Last year at ITC, Gadi Singer [VP and GM of Intel's mobility group] in a keynote speech said it's getting more and more difficult to provide test capabilities." Roddy then added, "Our design capabilities are outpacing our test capabilities, and we've got to have some changes in test."

"Our design capabilities are outpacing our test capabilities, and we've got to have some changes in test."
Paul Roddy

Roddy, who serves as co-chair of the STC University Working Group (UWG), said a key effort of the group is the alignment of goals: "Our member companies want to make sure that academia is working on projects that will be transferred to industry. Within the STC we have a lot of clout—with more than 30 member companies—and we can go to government agencies and say, 'this is really an important research project, and we need to get funding for it.'"

Getting a tester on campus, however, represents only a part of the picture. Roddy noted that an on-campus tester might get used only 10% of the time. Singh elaborated, saying "To maintain a test facility requires a full-time staff. It's possible to get a two- or three-year grant, or to get a piece of equipment donated, but it's very hard at a university to get a position or multiple positions funded for support staff. That's been part of the reason why donations sit there and gather dust."

Auburn is taking a multifaceted approach to make sure its tester doesn't gather dust. Singh said Auburn plans to open up the tester to other universities, whose researchers can log on over the Internet. Also under consideration, Singh said, is the hiring of a support person who could offer classes to commercial test-equipment users. "We could send our customers to Auburn for training," Roddy noted.

Yet another facet in the process of effectively using an on-campus tester is getting access to real-world wafers. Manufacturers, said Roddy, "don't like to give you bad devices, which are what you need to try out your test algorithms." Singh noted that even wafers that are a technology node or two old but that manufacturers would be willing to share would be helpful.

The Auburn initiative shows that universities are doing their part to align industrial and academic goals. Now's the time for industry to do its part by providing the wafers and data the university researchers need to ensure that test keeps pace with design.

Accompanying the online version of this editor's note is an edited transcript of my interview with Roddy and Singh, where they elaborate on Auburn's role in test research and on an open-architecture tester's advantages in a university environment (www.tmworld.com/2008_12). T&MW

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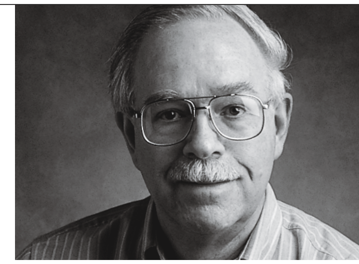
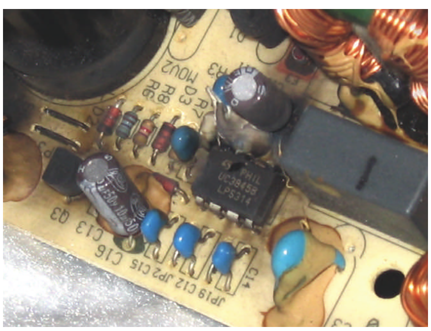


Make mine melamine

Long-time readers of this column may recall that I serve as a volunteer at WinCycle.org, a nonprofit computer-recycling center. When possible, we refurbish PCs for reuse by other nonprofit organizations and to provide operating revenue. One recent arrival from a local business contained a shipment of several hundred HP Compaq d530SFF desktop PCs, some of which exhibit an interesting and spectacular failure mode.

Applying AC power by plugging in the power cord produces a muted "pop" and a flash of light, followed by the release of a small puff of smoke—all originating from the PC's power-supply subassembly. Removing the power supply's cover reveals several severely damaged components. When the fault occurs, a soldered-in AC line fuse doesn't always open.



In an effort to learn more about the failure mode and label codes that might reveal affected manufacturing lots, WinCycle's CTO contacted Compaq's (now Hewlett-Packard's) online technical support service. Repeated and escalated message exchanges garnered no information, except for denial that the problem exists.

The power supply's construction comprises discrete through-hole components mounted on single-sided printed-circuit boards. A sheet-metal enclosure protects the assembly, and a small fan provides cooling (and smoke) dispersal. The power supply's label bears several safety-agency approval and recognition symbols.

The power supply's Chinese manufacturer applied generous amounts of an eggshell-colored and porous sealant to stabilize components mounted on the circuit board. The sealant darkens with exposure to heat and time. It also becomes conductive, creating multiple sneak paths among components. Inserting an ohmmeter's prods in random globs of sealant shows resistances in the 1-to-10-MΩ range. That's enough to inject small amounts of AC into the primary-side switching components and cause uncontrolled circuit activity.

We've reverse-engineered portions of the power-supply circuitry and determined that Revision B (or higher) power supplies contain a white sealant that's presumably nonconductive. To date, these power supplies haven't exhibited the failure mode.

What's in the conductive sealant? Given recent news reports about contaminated Chinese medicine and milk, my guess is melamine. What's yours? T&MW

KABOOM!

Brute force sometimes trumps subtle measurements. Without access to the manufacturer's original test criteria, we can't plan a test program for the Compaq d530SFF's model PDP124P power supplies. Instead, we're going to blow them up.

We'll assemble a simple timer and relay circuit to deliver AC to a group of supplies for a hundred or so on-off cycles. Power supplies that fail will get scrapped, and survivors will get disassembled and inspected for their (presumably) nonconductive sealant. We'll record the survivors' production-lot numbers and submit them to extended life tests.

Salvaging an unexploded power supply requires disassembly, removal of the tenacious conductive sealant, and replacement of potentially overstressed components. We don't have enough volunteers to perform repairs, nor does component cost and demand for these older PCs render repairs economical.

Would tests ferret out defective supplies? Probably not—the supply's input-filter components already draw leakage current from the AC line. Also, the destructive failure mode may manifest itself only at full line voltage. Will an exploding power supply cause a fire hazard? Probably not—sheet metal encloses the explodable components. Besides, a technician will oversee the festivities. For good luck, we'll keep a fire extinguisher handy.

No one can test "quality" into a marginal product. Tests can weed out the immediate failures, and short of a magic wand, that's the best we can hope for.

This YouTube video clip from an unknown source shows a Compaq d530's power-supply failure:

www.youtube.com/watch?v=nHPf6jHdEFg

This Web site offers instructions for removing, repairing, and replacing Compaq's PDP124P power supply:

webdevsys.com

Advantest debuts analog IC and memory test systems

Advantest recently introduced the 266-MHz T5782 memory test system for MCP/flash devices and memory-embedded microcontrollers, while the company's Kyushu Systems subsidiary has announced the ADS1911 test system for low-pin-count analog devices (**pictured**).

The T5782 memory test system provides 266-MHz/533-Mbps performance and targets flash memories as well as devices with memory-embedded microcontrollers. It can test KGD (known-good die) and MCP (multichip package) memory devices. The T5782 system can simultaneously test up to 256 devices and provides the performance of its predecessor, the T5781, with a footprint half the size. The T5782 also incorporates flash functions such as ECC (error checking and correction) and block management. Like the T5781, the T5782 offers both flash memory and DRAM test capabilities, enabling MCP test in addition to flash memory wafer and package test. Test programs developed on the company's T5781ES (engineering station), a tester designed for lab use, can be used for wafer test on the T5782 and for volume production on the T5781. Base price: 77 million yen.

The ADS1911 analog test system offers low-cost test for comparatively low-pin-count analog ICs (up to 32 pins), and it supports parallel test of up to eight discrete devices and analog ICs. To ensure accurate DC test, the ADS1911 is equipped with a DC calibration function that allows for minimal performance gaps between multiple installed systems, improving yield and bringing down cost. The system's test-program creation tool allows users to select test parameters from pull-down menus, eliminating the need for knowledge of specialized programming languages. Depending on configuration, the system can deliver voltages to ±128 V and currents to ±64 mA; it can also deliver 2-A pulse currents. Base price: 10 million yen. www.advantest.com.

Rohde & Schwarz announces earnings

Rohde & Schwarz celebrated its 75th anniversary in November, with executives expressing confidence in the future despite the economic crisis facing the world. While noting that no company is immune to economic disruption, president and CEO Michael Vohrer said that Rohde & Schwarz is well-positioned with its product offerings.

Announcing a net revenue of 1.4 billion euros for the past fiscal year (July 2007 to June 2008), Vohrer reported that the company achieved a year-end result comparable to the result for the previous year. Altogether, the electronics group has four main areas of business: test and measurement, secure communications, broadcasting, and radiomonitoring and radiolocation. The company says it was able to sell more instruments, particularly in the test and measurement and broadcasting fields, and that it continued to expand internationally, as evidenced by the regional headquarters it established in Singapore this past year.

"The entire economy is currently in a difficult situation, one in which it is important to practice entrepreneurial caution," Vohrer said. "We are therefore keeping a close eye on what occurs on the market, and we are applying a mixture of measures for promoting growth and reducing costs." www.rohde-schwarz.com.

Fujitsu chooses Keithley system

Keithley Instruments reports that it is developing a production test system for two 802.16e WiMAX devices from

Editors' CHOICE

Design your own PXI module

National Instruments has merged its LabView FPGA development software with a PXI module to create a platform for custom testers. The company's FlexRIO platform puts an FPGA on a PXI card. You can develop your own test module by programming the card's Xilinx FPGA with LabView to perform signal processing or to analyze serial data protocols. Through LabView FPGA software, you can gain access to 66 differential digital signals on the FPGA that run at speeds up to 1 Gbps. For single-ended operation, you get 132 pins at speeds up to 400 Mbps.

The PXI module needs an adapter card that connects your signals to the FPGA. Currently, NI provides a digital adapter (NI 6851) that lets you connect 54 single-ended channels to the FPGA. Voltage levels include 1.8 V, 2.5 V, and 3.5 V (5-V compatible). The NI 6851 adapter can transfer signals at 100 MHz, which means you can test DDR (dual-data rate) memory at 200 MHz.

Base prices: NI FlexRIO FPGA modules—$2999; NI 6851 adapter module—$999; FlexRIO development kit—$4999. *National Instruments, www.ni.com.*

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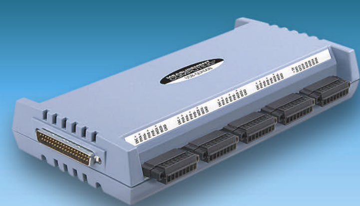

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Fujitsu Microelectronics. The manufacturing test setup, which features Keithley's Model 2820 RF vector signal analyzer and Model 2920 RF vector signal generator, will enable Fujitsu to perform a set of Tx and Rx test sequences and also test WiMAX devices in both SISO (single input, single output) and MIMO (multiple input, multiple output) modes. The system can generate MIMO signals with under 1 ns of timing alignment and less than 0.1° of phase jitter.

"WiMAX is quite possibly the most complex modulation scheme in the world, encompassing multiple technologies, and this complexity has made testing a challenge for manufacturers," said Mark Hoersten, VP of business development for Keithley. "Keithley's WiMAX test solution will enable Fujitsu Microelectronics to test in any frequency band between 400 MHz and 6 GHz faster and more easily than any competing offering." www.keithley.com; www.fujitsu.com.

Testronic tests WUSB products with Tek system

Tektronix has announced that Testronic Laboratories will be using the Tek UWB WiMedia compliance test solution to provide WUSB (wireless universal serial bus) interoperability testing at its test and certification centers. The UWB WiMedia system comprises the AWG7000 arbitrary waveform generator, the TDS6154C oscilloscope, and UWB (ultrawideband) spectral analysis software. Testronic Labs has been accredited by the USB Implementers Forum as an Independent Test Lab for testing and certification of WUSB products.

"Testronic Labs is the first test laboratory in Europe to be accredited to provide compliance testing and certification services for WUSB products and we are delighted that they chose our products to achieve this capability," said Lynne Camp, VP, Performance Products, Tektronix. www.tektronix.com; www.testroniclaboratories.com.

CALENDAR

OFCNFOEC, March 22–26, San Diego, CA. Managed by the Optical Society of America. www.ofcnfoec.org.

Measurement Science Conference, March 23–27, Anaheim, CA. Sponsored by Measurement Science Conference. www.msc-conf.com.

APEX, March 31–April 2, Las Vegas, NV. Sponsored by the IPC. www.goipcshows.org.

The Vision Show, March 31–April 2, Phoenix, AZ. Sponsored by the Automated Imaging Association. www.machinevisiononline.org.

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Test, inspection products introduced amid economic uncertainty

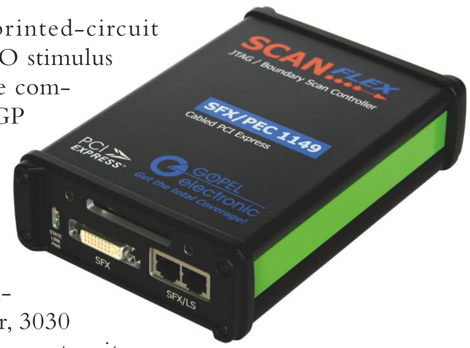
> > > Electronica 2008, November 11–14, Munich, Germany, www.electronica.de.

The attendance for electronica 2008 was remarkably stable despite the difficult financial situation facing many exhibitors and attendees, announced show organizer Messe München International. Messe München added that the trade fair attracted around 2800 exhibitors and around 72,000 attendees—numbers essentially unchanged from the previous electronica show in 2006.

On the show floor, **Rohde & Schwarz** debuted its FSH4 and FSH8 handheld spectrum analyzers and said it has added microwave models to its FSV family of benchtop signal and spectrum analyzers. **Goepel electronic** introduced the 9305-BAC/Bluetooth bus access cable—a new member of the ScanFlex boundary-scan product family. Goepel also debuted new SFX/PEC 1149 ScanFlex controllers, its OptiCon X-Line 3D in-line 3-D x-ray inspection system, and, in cooperation with **Texas Instruments**, VarioTAP emulation technology in the form of a model library for TI's TMS320C2000 platform.

JTAG Technologies introduced the multi-programmable-voltage JT 2149/MPV DIOS (digital I/O scan) module, which allows digital I/O test access to PCBs (printed-circuit boards) requiring external I/O stimulus and response monitoring. The company also said its JT 2147/AGP boundary-scan interface works with **Aeroflex** ICTs (in-circuit testers). For its part, Aeroflex announced it has added to its PXI Modular Instrument 3000 Series an embedded PXI system controller, 3030 Series GSM/EDGE measurement-suite enhancements, and two new AWG (arbitrary waveform generator) memory options.

Digitaltest debuted its QMAN SQL database, which supports visual inspection and functional test. **Aster Technologies** highlighted TestWay software, which analyzes electrical testability requirements and estimates test coverage aligned to specific PCB test strategies. **Viscom** debuted its EasyGen automated-optical-inspection program-generation tool, which can work even with incomplete PCB CAD data. The company also highlighted its S6053BO-V fully automatic wire-bond inspection system, which supports resolutions down to 2 to 5 microns per pixel. T&MW



The SFX/PEC 1149 controllers, available in three performance classes, comply with the PCI Express external-cabling specification.
Courtesy of Goepel electronic.

CAST established as test products debut

> > > International Test Conference, October 28–30, Santa Clara, CA, www.itctestweek.org.

At this year's ITC, representatives of nine companies—**Advantest, Amkor, Infineon, Intel, LTX-Credence, Qualcomm, Roos Instruments, Teradyne,** and **Verigy**—came together under the CAST banner in an effort to foster pre-competitive collaboration. CAST, which stands for Collaborative Alliance for Semiconductor Test, will work to resolve common industry issues with the goal of achieving higher equipment utilization, easier line balancing, and greater return on investment for equipment users.

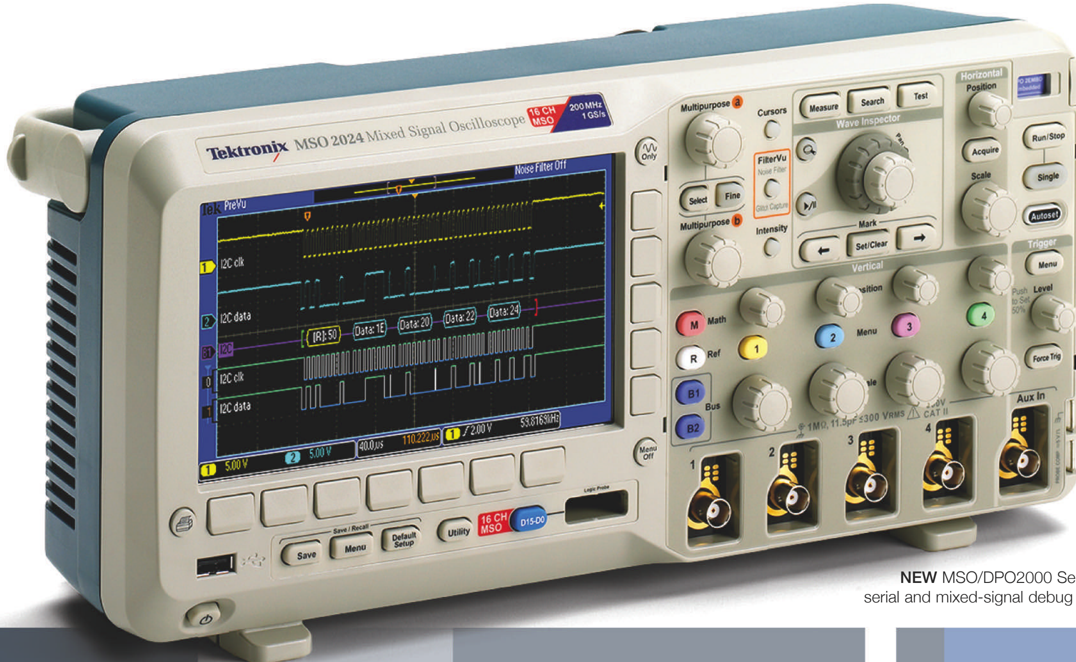
Goepel electronic introduced the SFX-9305 I/O module as a new addition to the ScanFlex hardware platform. The company also announced extended JTAG functionality for the SPEA 4040 flying prober. **Asset InterTech** said it has joined **Synopsys**'s in-Sync program for third-party suppliers of EDA-related products. Asset also highlighted its RIC (Remote Instrumentation Controller) family.

Cadence Design Systems said **Hitachi** has combined Encounter Test pattern-fault modeling with test pattern generation, compression, and diagnostics to produce LSI devices for telecommunications and other applications. Cadence also said that **Moai Electronics** has deployed Cadence Encounter RTL Compiler and Encounter Test to successfully tape-out a flash memory controller. Representatives of **JTAG Technologies** and **Teseda** were on hand to describe separate initiatives in conjunction with **Teradyne** that involved TestStation boundary-scan integration and silicon debug, respectively.

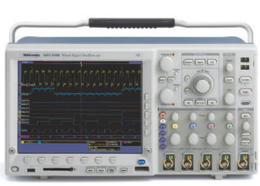
OptimalTest said that it has signed an agreement with **STATS ChipPAC** to provide OptimalTest's Station Controller software as a test-management tool. **Intellitech** introduced its UltraTAP-BT, a Bluetooth-enabled IEEE 1149.1/JTAG pod with nonvolatile test program and failure memory. T&MW

Overachiever.

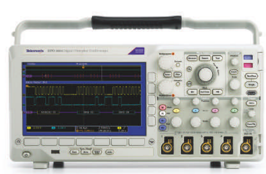
NEW mixed-signal scope series with advanced features starting at $2580...



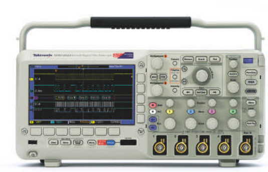
NEW MSO/DPO2000 Series with serial and mixed-signal debug features



MSO4000/DPO4000 Series	
Bandwidth	350 MHz to 1 GHz
Analog Channels	2, 4
Digital Channels	16 (MSO4000 Series)
Record Length	10 M on all channels
Display	10.4 inch
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN, FlexRay



DPO3000 Series	
Bandwidth	100 MHz to 500 MHz
Analog Channels	2, 4
Digital Channels	—
Record Length	5 M on all channels
Display	9.0 inch
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN



NEW! MSO2000/DPO2000 Series	
Bandwidth	100 MHz to 200 MHz
Analog Channels	2, 4
Digital Channels	16 (MSO2000 Series)
Record Length	1 M on all channels
Display	7.0 inch
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN

At that price point, you'd expect the new addition to the MSO/DPO family to have modest goals. Don't tell that to the MSO/DPO2000 Series. You see, with up to 200-MHz bandwidth, 1 GS/s sample rate, and as many as 4 analog and 16 digital channels, it's more than ready for mixed-signal debug. It even offers advanced features like Wave Inspector® for navigating long records and automatic decode of serial buses just like the other members of the family, the DPO3000 and MSO/DPO4000 Series. With a heritage like that, the MSO/DPO2000 Series is sure to exceed expectations.

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MARTIN ROWE
SENIOR TECHNICAL EDITOR
m.rowe@tmworld.com

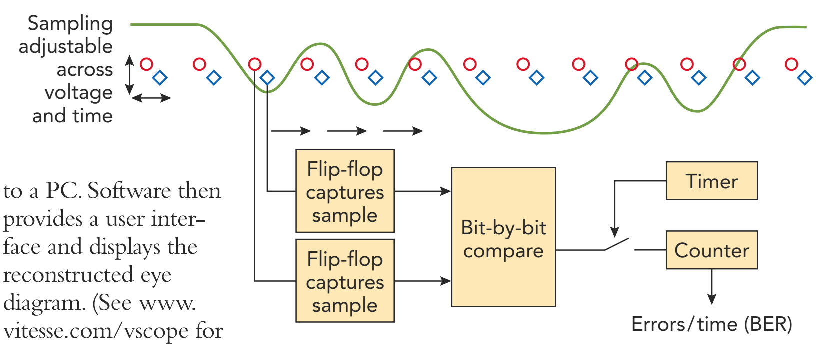
On-chip testers gain momentum

With today's communications ICs running serial buses at multigigabit rates, knowing what's going on inside the package is becoming essential. Two IC makers, Vitesse and PLX Technology, have solved the problem by embedding testers into their parts. In both cases, the embedded testers arose from a need for the companies' engineers to debug their devices. Soon, the companies found customers were asking for the testing technology.

Vitesse started several years ago with what is now VScope, which is essentially an equivalent-time-sampling digitizer. Product manager Juan Garza explained that while developing a CDR (clock-data recovery) circuit, engineers needed to view the high-speed signals after they were equalized inside the chip. Conventional test equipment has access to IC pins, but not to the inside of the package. At the time, data rates were 1–2 Gbps. Now, with data rates at 10 Gbps and faster, Vitesse engineers can't live without VScope.

The **figure** shows how VScope works. It samples a waveform at two points. At the center of the eye, a fixed-position sampler digitizes voltage. At another location—this one can vary across the eye—VScope also samples the signal. From the sampling points, VScope calculates BER (bit error rate). From the difference in BER, PC software can reconstruct the signal eye.

The IC has an SPI (serial peripheral interface) bus from which the device sends the sampled data. A development board converts the SPI signals to USB (universal serial bus) format for transport to a PC. Software then provides a user interface and displays the reconstructed eye diagram. (See www.vitesse.com/vscope for more information.)



VScope samples incoming signals with an on-chip digitizer. Courtesy of Vitesse Semiconductor.

PLX Technology develops and manufactures switch ICs for PCIe (PCI Express). PCIe is a packet-based protocol, and PLX engineers wanted to decode it to determine when a link was established. Instead of using external test equipment, which consumed bench space, the engineers designed a PCIe packet generator and analyzer into the ICs. "We could figure out what was happening with a logic analyzer," said principal architect Jeff Dodson, "but we were unable to connect external test equipment to all 24 ports on a switch."

Dodson has written a paper that explains how the PCIe on-chip exerciser and analyzer works. You can download it from the online version of this article (www.tmworld.com/2008_12). In a nutshell, the packet generator mimics the ingress stream of TLPs (transaction-layer packets). It can saturate a PCIe Gen2 link in both directions so you can test each lane at full capacity.

The PCIe packet analyzer is independent of the exerciser. It can monitor PCI data streams and keep count of memory reads, memory writes, and completions, all of which are the PCIe bus transactions.

Like VScope, the PCIe generator and analyzer communicates to a host PC through the IC's I^{2}C bus, converted to USB by an evaluation board. PC software provides a user interface where it plots the data. The online version of this article includes a screen image of the PCIe analyzer.

Both companies have found that their customers use the on-chip testers not only when developing products with the ICs, but also when testing deployed systems. In fact, Garza noted that "we have trouble convincing customers to return the evaluation boards." T&MW

Application note discusses signal integrity in networks

"A Design of Experiments for Gigabit Serial Backplane Channels" from Agilent Technologies discusses measurements of high-speed backplane interconnects. The paper covers test setups using a VNA (vector network analyzer) for measurements such as eye diagrams, impedance, insertion loss, and crosstalk. cp.literature.agilent.com/litweb/pdf/5989-8864EN.pdf.

USB server connects devices over wireless network

With the USBN-500W from Quatech, you can connect USB devices such as data-acquisition systems, oscilloscopes, and DMMs (digital multimeters) over an IEEE 802.11 wireless network. The server can accommodate 14 USB devices, with itself as a hub. www.quatech.com.

The "must have" wireline network reference

The "Must Have Reference for IP and Next Generation Networking" from Anritsu is a free reference for the IEEE 802.3 series of Ethernet standards and acronyms. This 57-page document helps you sort out what's what in wireline networks. www.us.anritsu.com/downloads/files/musthave.pdf.

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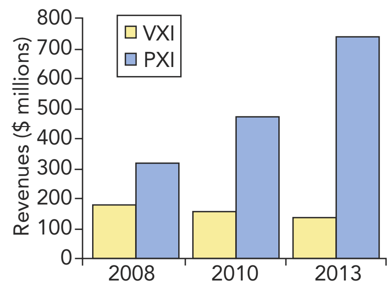
Competing bus technologies continue to coexist

Since the introduction of PXI in 1997 by National Instruments, several concerns have been raised by end users and suppliers about the future of VXI. Having been around for over two decades, and with more than 80 vendors offering over 1200 commercial VXI products, the VXI platform has successfully endured the test of time and continues to retain a share of the modular test market (see **figure**).

Aerospace, military, and defense continue to be the largest user segment for VXI. VXI's large installed base in this segment is attributed to the fact that it was the first industry standard for modular instruments. As a result, it saw widespread adoption during the early 1990s. Aerospace, military, and defense industries require test equipment that can be supported over the long term, typically 15 to 20 years, to match the long life spans of military and aerospace equipment. VXI systems developed during the 1990s remain in use, and new test systems are still built around VXI, especially for high-density, high-performance, high-channel count applications in the military and aerospace market, which expects to sustain demand for VXI test equipment in the future.



Projected world market revenues by product type for the VXI/PXI test equipment market from 2008 to 2013.

In spite of VXI's resilience, PXI is now penetrating low-end applications in the ATE (automated test equipment) and functional test and measurement areas in the aerospace, military, and defense markets. Customers are beyond the early adoption stage and are looking forward to improved functionality to address increasingly sophisticated applications. The revenues for PXI equipment are expected to more than double over the next five years.

One of the most dynamic applications for PXI is its use in the testing of complex, high-bandwidth RF applications. PXI is increasingly becoming mainstream in RF applications and has made rapid strides to penetrate the telecommunications, military, aerospace, and avionics markets. The rapid explosion of cellphones and the evolution of technologies such as WiMAX, UMTS, CDMA, TD-SCDMA, GSM, GPRS, EDGE, and LTE have offered tremendous opportunities for the PXI market, as these applications require a form factor that provides flexibility and a high price-performance ratio. In addition, the PXI Express specification provides high bandwidth to target high-speed digital applications such as video-streaming, machine-vision, and semiconductor ATE applications.

When LXI was introduced in 2005, there were concerns once again across the industry. This time around, VXI and PXI vendors are not worried about being phased out. They look to adapt and provide solutions on how to integrate these instruments into their systems. The proliferation of modular instrumentation offers an opportunity as well as a challenge to system developers. Besides, history has taught us that they will likely continue to coexist, as each technology has its own merits and is suited to different applications. T&MW

PCB book-to-bill

For rigid PCBs (printed-circuit boards) and flexible circuits combined, industry shipments in October 2008 decreased 4.8% from October 2007 and orders booked decreased 14.6% from October 2007. Year to date, combined industry shipments are up 3.6% and bookings are down 2.5%. The combined (rigid and flex) industry book-to-bill ratio in October 2008 increased slightly to 0.96. The book-to-bill ratio for the North American rigid PCB industry in October 2008 slipped slightly to 0.95. The flexible circuit book-to-bill ratio in October 2008 jumped up to 1.00. www.ipc.org.

Semiconductor equipment book-to-bill

North American-based manufacturers of semiconductor equipment posted $843 million in orders in October 2008 (three-month average basis) and a book-to-bill ratio of 0.93. The bookings figure is about 30% greater than the final September 2008 level of $650 million, and about 28% less than the $1.18 billion in orders posted in October 2007. The three-month average of worldwide billings in October 2008 was $908 million. www.semi.org.

HDMI grows while DVI slides

The rapid rise of HDMI (high-definition multimedia interface) and the slow decline of DVI (digital visual interface) continued in 2008, reports In-Stat in the $3695 report "DVI and HDMI 2008: A Time of Transition." The primary driver of HDMI's success is the consumer segment, with HDMI ports being found on 95% of the digital televisions shipped worldwide in 2008, the greatest volume for HDMI in any product, the high-tech market research firm says. The vast majority of DVI shipments occurred in PC and PC-peripheral markets. DVI and HDMI are related, high-bandwidth, unidirectional, uncompressed digital interface standards. www.in-stat.com.

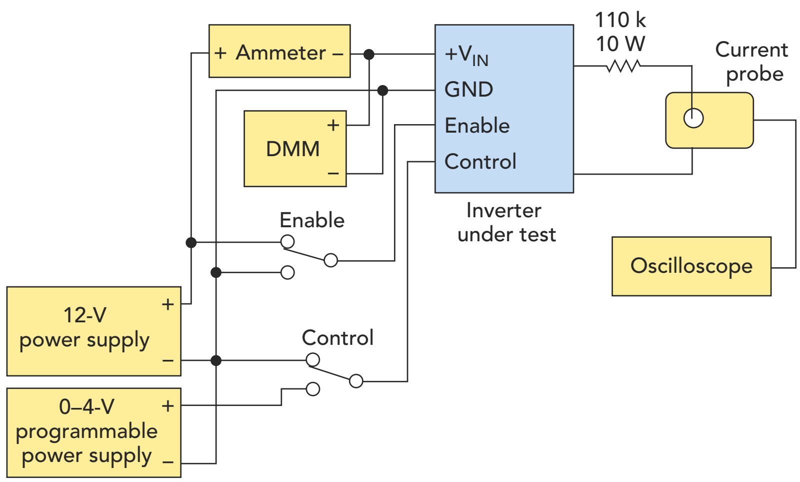
INSTRUMENTS

Testing inverters for backlighting

CCFLs (cold cathode fluorescent lamps) provide backlight for many kinds of displays. To get CCFLs started, a DC-to-AC inverter must produce 1000-VAC to 2000-VAC RMS from DC voltages between 5 V and 12 V. After the CCFL illuminates, the inverter must supply from 500 VAC to 1000 VAC RMS to keep the light shining.

Manufacturers of DC inverters must test them for input current and voltage, output current and voltage, output frequency, and power efficiency. Engineers at Endicott Research Group design such inverters and have developed an automated test station for production use. Endicott Research president Tom Novitsky and engineering manager Bob Arnold have written a paper that describes the inverter and test station in detail. You can download the paper from the online version of this article (www.tmworld.com/2008_12).

The test station (**figure**) consists of two power supplies, an oscilloscope, a current probe, and two DMMs (digital multimeters). The 12-V power supply provides power for the inverter, and the 0- to 4-V supply provides a control voltage for setting the inverter's output. A PWM (pulse-width modulator) in the inverter varies its duty cycle based on the control voltage to control the lamp's brightness.



DC inverters convert DC to AC and require testing for input and output current and voltage.

Test operators use the oscilloscope to measure output current and frequency. They use the DMMs to measure input voltage and current. A PC calculates power efficiency and stores test results for each inverter on the company LAN.

Martin Rowe, Senior Technical Editor

COMPLIANCE

RoHS standards present moving target

One challenge to ensuring that electronic products conform to industry regulations is that those regulations often seem arbitrary. Just when companies think they have made sufficient plans to conform, the rules change. As a case in point, the European Union is considering revising the RoHS (Restriction of Hazardous Substances) directive so it covers products such as medical devices and industrial-monitoring equipment and also bans many more chemicals from use in electronics products. Unfortunately, according to a white paper recently released by IPC, implementing some of those changes unaltered could cripple the electronics manufacturing industry.

For example, the EU is proposing a ban on halogen-based chemicals such as TBBPA (tetrabromobisphenol[a]), a flame retardant used in PCB (printed-circuit board) laminates in some two-thirds of the electronic appliances worldwide. In its paper, the IPC contends that there is no evidence of harmful effects from the chemical when it is used in the epoxy resins of PCBs and that there is no adequate universal substitute.

The IPC paper also argues that a ban on this material would have significant side effects. Although halogen-free alternatives are available, quantities are limited, and their inclusion would raise manufacturing costs dramatically (see "Costs of TBBPA ban as estimated by the IPC," p. 24). Costs aside, these materials have not undergone the rigorous risk assessments that TBBPA has, and the phosphorus and other elements that they contain may turn out to be more toxic than the bromide that they are intended to replace. Some products would not tolerate the substitution at all.

Another of the proposed regulations suggests doing away with "all organic compounds containing chlorine and bromine," an action that would create even more havoc, according to the IPC. The original RoHS directive banning lead from electronic solder caused considerable pain as the industry scrambled to find a suitable replacement. The new lead-free solders have a higher melting point than their predecessors did and permit much narrower process conditions during PCB manufacture.

The proposed revisions to the directive would aggravate the situation. Plasticizers and wetting agents used in solder include compounds that would fall under the new ban. Most solder fluxes also contain halides, and there are currently no viable alternatives. In addition, the regulation's ambiguous wording could leave manufacturers unsure of whether their processes conform.

The white paper insists that demanding the industry to replace compounds that have endured years of validation for their intended use with untried and untested alternatives risks system failures, with consequences ranging from mild annoyance to the catastrophic result of an avionics or medical electronics failure. See the online version of this article at www.tmworld.com/2008_12 for a link to the IPC paper, "The Electronic Interconnection Supply Chain's Response to Öko-Institut's Recommendations for Proposed Revisions to the RoHS Directive."

Steve Scheiber
Contributing Technical Editor

Costs of TBBPA ban as estimated by the IPC

- Substitution with a halogen-free alternative would add $211 million per year in material costs.
- The approval cycle for PCB makers would take from two to five years and cost another $17 million to $21 million per year.
- The ban would require a redesign of many boards, with unpredictable consequences in both cost and performance.
- For some products, a halogen-free alternative doesn't exist, and developing one could take five years or more.
- Products that require additional approvals (such as medical products that need FDA approval in the US) would require additional years of testing.

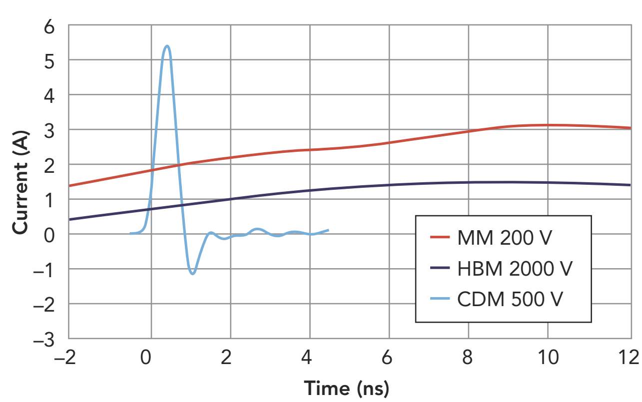
Source: "The Electronic Interconnection Supply Chain's Response to Öko-Institut's Recommendations for Proposed Revisions to the RoHS Directive."

A version of this article appeared in the *EDN Global Innovators 2008* supplement to the November 13 issue of *EDN*.

ELECTROSTATIC DISCHARGE

ESD tests generate different results

Whenever an electrically charged object discharges, it produces an ESD (electrostatic discharge) event. An ESD event can subject an electronic device to thousands of volts and several amperes. High voltage can cause a breakdown in a device structure, and high current can generate heat that damages the device.



Charged device model tests produce higher current (light blue trace) than do human body model (dark blue trace) or machine model (red trace) tests.

The current discharged into a device depends on the ESD voltage and on the characteristics of the device's current path. But the amount of current that passes *through* a device differs drastically for a given discharge voltage, depending on the test method you use. Unfortunately, the reasons why current differs for a given voltage are not always well understood.

"ESD Device testing: The test determines the result," a paper by Robert Ashton, senior protection and compliance specialist at ON Semiconductor, explains that the amount of current that can pass through a device depends on the test you apply to it. The paper covers the three test methods—HBM (human body model), MM (machine model), and CDM (charged device model)—by showing each model's test circuits, which are designed to produce consistent test results.

"CDM produces a much shorter current pulse than either HBM or MM, but it produces a substantially higher peak current," notes Ashton in the paper. "HBM and MM can deliver more energy to the device under test, but high peak currents are often the best predictor of damage."

Using waveform plots on different time scales, Ashton shows the differences in each model's waveform. The paper also compares the current waveforms produced by tests that comply with two ESD system-level test standards, IEC 61000-4-2 and ISO 10605, which use different resistor and capacitor values in their test circuits. The online version of this article (www.tmworld.com/2008_12) contains a link to the paper.

Martin Rowe, Senior Technical Editor

More measurements. More data. Less cost.

With up to 560 channels of data logging at a maximum scan rate of 1000 channels/sec, an internal 6 ½ digit DMM with 22-bit resolution, and 0.03% accuracy, it's no mystery why Agilent's data acquisition systems are among the top selling in the world. The 34970A and 34980A are both at home with either data acquisition or functional test, with a broad selection of plug-in modules.

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Produce AC test signals

Use this circuit as a DC-biased AC source when you need both low-distortion and power driving capability.

By Tiger Zhou and Robert Dobkin, Linear Technology

AC testing of electronic systems often requires a low-distortion signal source to excite a DUT (device under test). Instead of using a signal generator and a power amplifier to produce a low-distortion AC signal, you can build a power oscillator with just one IC and a few discrete components.

Figure 1 shows a power oscillator that uses a twin-T filter network and a high-power LDO (low dropout) regulator to produce a DC-biased AC signal. The LDO regulator's op amp and output transistor form a voltage follower. A precision 10-μA current source and the R_{SET} resistor set the circuit's DC-level output.

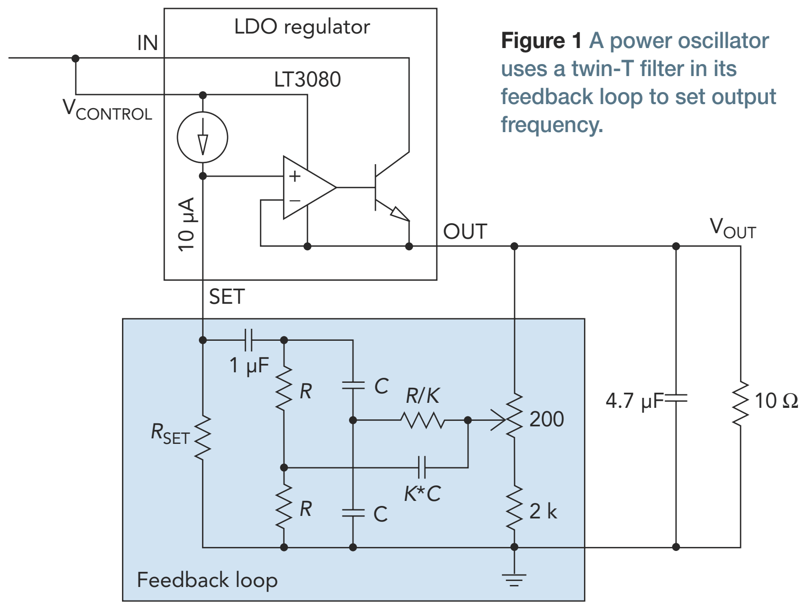

Figure 1 A power oscillator uses a twin-T filter in its feedback loop to set output frequency.

Oscillation begins when positive feedback is present in the loop. The oscillation will be stable when the loop gain is unity. When the loop gain is greater than unity, the oscillation amplitude will keep increasing until the components saturate. When the loop gain is less than unity, the oscillation will diminish. A feedback potentiometer lets you adjust the loop gain so it is close to unity, which maintains a stable oscillation.

A notch filter in the feedback loop, made from two T-type filters in parallel (one low-pass, one high-pass), sets the oscillator's output frequency. The LDO regulator then amplifies the signal and drives the load.

The twin-T notch filter in the feedback loop between the OUT pin and SET pin attenuates frequencies above and below the filter's center frequency (f_0), which is the oscillator's output frequency. Using the equation below, you can calculate values of resistors and capacitors to get f_0. For f_0 = 400 Hz, R = 8.45 kΩ and C = 47 nF.

$$f_0 = \frac{1}{2\pi RC}$$

At f_0, the twin-T network's gain is maximized near unity. The maximum gain, though, changes with the value of K in Figure 1. When $K = 2$, the oscillator's maximum gain is 1.0 (**Figure 2**). When $K = 5$, the gain increases to 1.1, and the gain decreases even more if K should become greater than 5. Thus, you should select a K value from 3 to 5 for a larger than unity gain, then attenuate the feedback signal with the potentiometer to achieve oscillator stability.

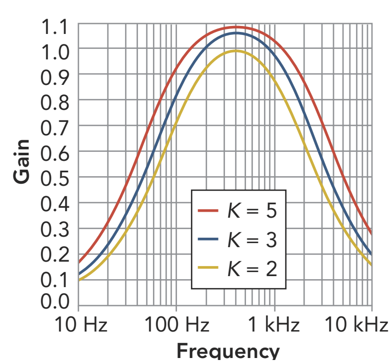

Figure 2 Loop gain changes with the value of *K* from Figure 1.

While the potentiometer will work, it will not provide automatic gain control; you can get that if you replace the potentiometer with a light bulb or a MOSFET. The online version of this article contains schematics for both implementations (www.tmworld.com/2008_12).

Because a light bulb heats when turned on, its resistance will increase with the oscillation amplitude. Thus, the bulb's change in resistance tunes the feedback loop's gain to maintain the oscillation. In the MOSFET implementation, a Zener diode detects the oscillator's peak voltage. The MOSFET's resistance decreases as oscillation amplitude increases, which decreases the oscillator's loop gain and maintains the oscillation.

Figure 3 shows the oscillator's signal output and harmonics using the light bulb in the feedback loop. With f_0 of the twin-T oscillator at 400 Hz, the circuit's THD (total harmonic distortion) is 0.1%. We also measured the circuit's performance at f_0 = 8 kHz. At that frequency, THD jumped to 7%.

(continued)

The most significant harmonic contribution comes from the second harmonic (lower trace), which is less than 4 mV_{pk-pk} in the light-bulb implementation. The online version of this article shows the oscillator's output and harmonics using the MOSFET implementation. With the MOSFET, the circuit's THD is 1% with a 40-mV_{pk-pk} second harmonic. The MOSFET's resistance changes more quickly and thus produces greater harmonic content than the light bulb.

When designing and using an oscillator, you must also consider the oscillator's dynamic response. The startup is one of the few criteria representing the oscillator's stability. The startup of a well-designed oscillator should have minimum overshoot and have no swinging of its output amplitude. Unlike many oscillators, both the light bulb and the MOSFET implementations maintain a constant peak-to-peak amplitude.

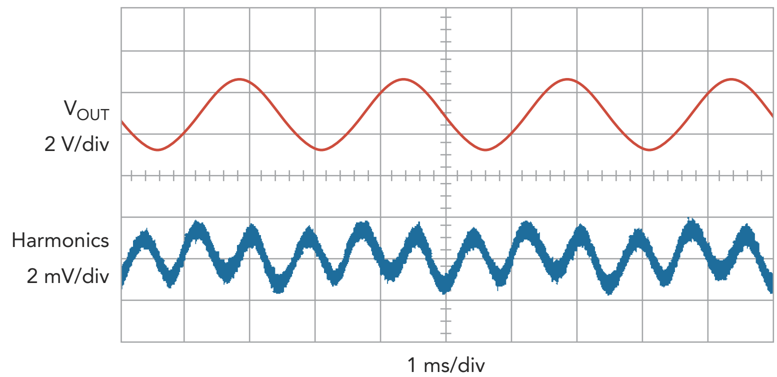

Figure 3 Using a light bulb in the oscillator's feedback loop produces a 400-Hz sine wave with low distortion for the second harmonic.

The twin-T oscillator can drive any type of load—inductive, capacitive, or resistive—with a drive capability up to 1.1 A, which is the limit of the LT3080 LDO. Your circuit's load will limit the maximum frequency that you can get from the oscillator while maintaining low distortion.

When testing the oscillators, we observed a very small amount of overshoot at startup. The MOSFET variation stabilizes faster than the light-bulb version because the latter has a long thermal constant caused by heating. T&MW

The authors would like to thank Tony Bonte, Mitchell Lee, Jim Williams, and Todd Owen for fruitful discussions.

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VOTE for the Best in Test 2009

Our editors have selected the finalists for the Best in Test awards and the Test of Time award.

Vote online for the winners by February 6, 2009: www.tmworld.com/awards

Test & Measurement World's editors have combed through many deserving products, nominated by vendors, that were introduced between November 1, 2007, and October 31, 2008. On the following two pages, we present the finalists for the 2009 Best in Test awards and ask you to help us choose the best of the best. Visit www.tmworld.com/awards to cast your vote for your favorite product in each of the 15 categories. We will announce the category winners on April 1 at www.tmworld.com and in our April issue. The overall top vote getter will be declared the 2009 Test Product of the Year.

We have also selected six finalists for the Test of Time award, which honors a product that continues to provide state-of-the-art service five years or more after its introduction. Help us choose the 2009 Test of Time winner by casting your vote for the finalist of your choice. The Test of Time winner will also be announced April 1.

Voting deadline: February 6, 2009.
www.tmworld.com/awards

2009 Finalists

Audio/video and multimedia

- **IxRave Service Validation Platform**
  Ixia
- **Multimedia Test System**
  VI Technology
- **PEVQ Analyzer**
  OPTICOM
- **WaveQoE Test Suite**
  VeriWave

Board and system test and configuration

- **Cover-Extend Technology**
  Agilent Technologies
- **Flashstream Flash Vector Programming System**
  BPM Microsystems
- **Flying Scorpion FLS900 Dx Flying Probe System**
  Acculogic
- **SigmaSure Process Flow Visualization Software**
  SigmaQuest
- **TS-375 Avionics Test Platform**
  Geotest—Marvin Test Systems

Boundary scan

- **JT 37x7 Rack-Mountable Instrument**
  JTAG Technologies
- **onTAP Series 4000 Software Featuring ProScan**
  Flynn Systems
- **Remote Instrumentation Controller 1000**
  ASSET InterTech
- **ScanBox RM System**
  Acculogic
- **UltraTAP-BT Test Pod**
  Intellitech
- **VarioTAP Platform**
  GOEPEL electronic

Data acquisition

- **DAC5682Z Digital-to-Analog Converters**
  Texas Instruments
- **DNR-12-1G Ethernet I/O Rack**
  United Electronic Industries
- **TEMPpoint Temperature Measurement Instrument for Ethernet (LXI)**
  Data Translation
- **USB-1616HS-BNC Multifunction Data Acquisition Device**
  Measurement Computing
- **Wi-Fi Data Acquisition Devices**
  National Instruments

EDA/DFx/Test data-analysis software

- **DFT MAX Compression Solution**
  Synopsys
- **Encounter True-Time ATPG**
  Cadence Design Systems
- **Global Test Operations Solution**
  OptimalTest
- **Solder Joint Built-In Self-Test Software**
  Ridgetop Group

General-purpose instruments (non-oscilloscopes)

- **287 True-rms Electronics Logging Multimeter**
  Fluke
- **86108A Precision Waveform Analyzer**
  Agilent Technologies
- **DPP12500A-4T 12.5 Gbps 4 Tap Digital Pre-emphasis Processor**
  Synthesys Research
- **NSG 3060 Immunity Pulse Testing System**
  Teseq
- **Precision Resistor Module Family**
  Pickering Interfaces
- **U1253A Handheld Digital Multimeter with OLED Display**
  Agilent Technologies

Machine vision and inspection

- **sprint Color Cameras**
  Basler Vision Technologies
- **Genie GigE Vision-Compliant Cameras**
  DALSA
- **In-Motion Measurement for WYKO 9000 Optical Profilers**
  Veeco Instruments
- **MV-7L In-line AOI System**
  MIRTEC
- **OptiCon TurboLine AOI System**
  GOEPEL electronic

Network physical-layer test

- **100GbE Development Accelerator System**
  Ixia
- **AXS-635 Triple-Play Test Set**
  EXFO
- **MW90010A Coherent OTDR**
  Anritsu
- **Precision Reflectometer 4400**
  Luna Technologies

Oscilloscopes

- **DLM2000**
  Yokogawa
- **DPO3000**
  Tektronix
- **InfiniiVision 7000**
  Agilent Technologies
- **M-Class**
  ZTEC Instruments

Read all about the finalists and cast your votes online at www.tmworld.com/awards. Voting deadline: February 6, 2009.

- PicoScope 9201
Pico Technology
- WavePro 7 Zi
LeCroy

Protocol analyzers

- IxYukon Load Module
Ixia
- N5309A-COM Compliance Assured Test Package
Agilent Technologies
- TestCenter 3000 Series Module
Spirent Communications
- Xgig FCoE Test Platform
Finisar

RF/microwave instruments: Application/standard specific

- 3500A Portable Radio Communications Test Set
Aeroflex
- BTS Master and Spectrum Master Analyzers
Anritsu
- DigRF V4 Exerciser/Analyzer
Agilent Technologies
- IQultra UWB Test System
LitePoint
- URT Record & Playback System 4.0
Averna

RF/microwave instruments: General purpose

- 6.6 GHz PXI Express RF Modular Instruments
National Instruments
- GT-1000A Microwave Power Amplifier
Giga-tronics
- Model 1830A RF Power Meter
TEGAM
- R&S FSV Signal and Spectrum Analyzer
Rohde & Schwarz
- SA2600 Handheld Real-Time Spectrum Analyzer
Tektronix

Semiconductor test

- Automated Contact Resistance Socket Tester (CR-2600)
Antares Advanced Test Technologies
- EDGE Flicker Noise Measurement System
Cascade Microtech
- MT2168 Pick and Place Service
Multitest elektronische Systeme
- Protocol Aware Test System
Konrad
- Turnkey RF Test Cell
Advantest
- UltraWave 12G Test Instrument
Teradyne

Test accessories and interconnects

- Edge 400a Series Contactors
Johnstech International
- Gemini Kelvin Spring Pins
Everett Charles
- Lead Free Test Probes
Interconnect Devices
- Synergetix Dyno Test Socket for QFN Devices
Interconnect Devices
- Ultra High Density (UHD) Interconnect Builder
W.L. Gore & Associates
- W2630A Series DDR2 and DDR3 BGA Probes
Agilent Technologies

Test-development and test-management software

- Arendar 2009 Suite
VI Technology
- Simics 4.0
Virtutech
- TestShell 2.2
QualiSystems
- UPC Manager
Pacific Power Source
- VEE Pro 9.0
Agilent Technologies

TEST OF TIME

Inaugurated in 2005, the annual Test of Time award honors a test, measurement, or inspection product that has provided state-of-the-art service for at least five years after its introduction.

2009 Finalists

ATEasy Test Executive and Development Environment
Geotest—Marvin Test Systems

Medalist 5DX Automated X-Ray Inspection System
Agilent Technologies

Pad ROL 100 Series Test Contactor
Johnstech International

PhaseFlex Microwave/ RF Test Assemblies
W.L. Gore & Associates

TDS3000 Series Oscilloscopes
Tektronix

TestKompress ATPG Tool
Mentor Graphics

Read all about this year's finalists and cast your vote at www.tmworld.com/awards

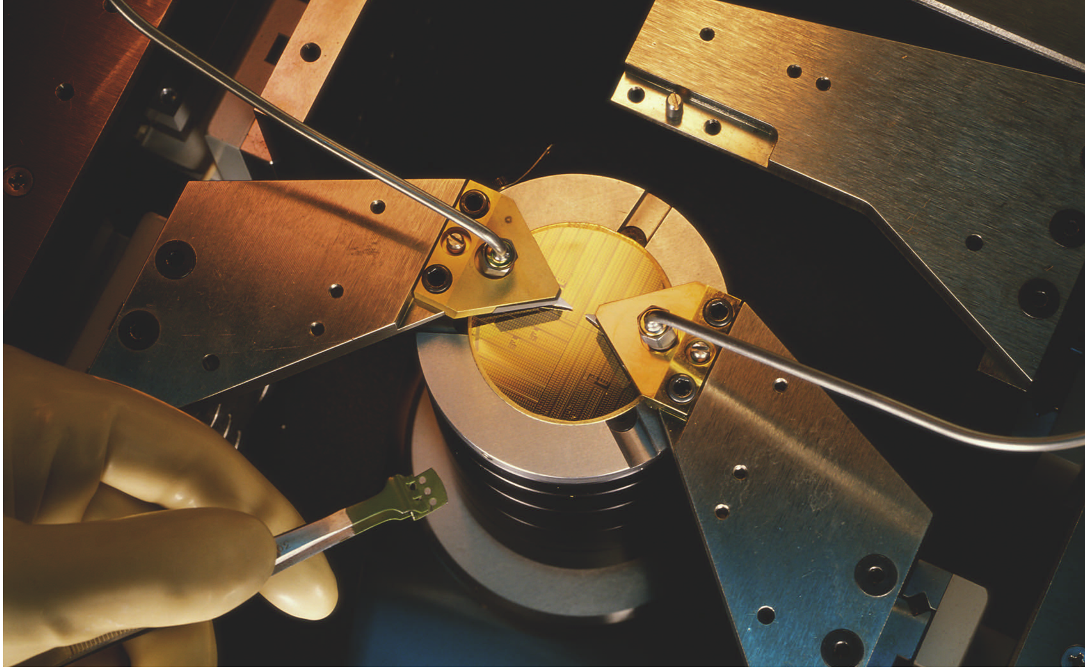
Past winners:

2008: DL750 ScopeCorder
Yokogawa

2007: LabView
National Instruments

2006: 2400 SourceMeter
Keithley Instruments

2005: 93000 System-on-Chip Tester
Agilent Technologies (now Verigy, formerly Hewlett-Packard)



Diagnosis-driven YIELD ANALYSIS

Shorten the path to finding the root cause of yield-limiting systematic defects for advanced IC designs.

BY DAVE MACEMON, MENTOR GRAPHICS

Numerous challenges have to be overcome during design and production of ICs below 90 nm. Manufacturing processes are still being characterized, and the interactions between the physical processes and design features can be extremely subtle and difficult to identify. As a result, meeting yield goals is a bigger challenge than it was at larger technology nodes, and this has a direct impact on profits. The faster a new design can be ramped up to volume production rates, the faster the time to profit (**Figure 1**).

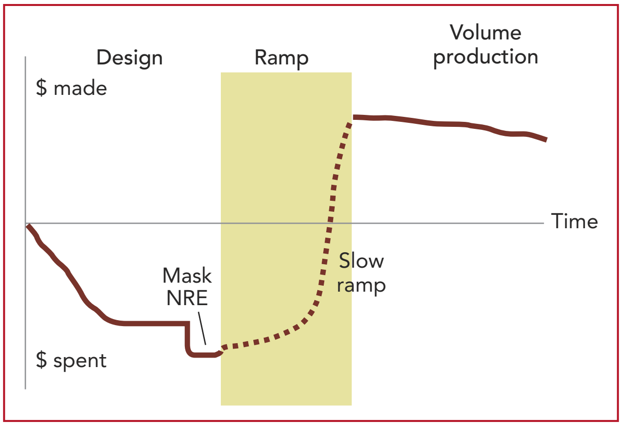


FIGURE 1. As this yield ramp shows, the faster a new design can be ramped up to volume production rates, the faster the time to profit.

Yield management has traditionally been the responsibility of one or more engineers who also are responsible for design, test, production, or processing. Once a design is in production, the yield manager's job is to make the product "yield better" by, among other things, identifying yield limiters and specifying changes to the design, test, or manufacturing process. Finding the root cause of yield-limiting defects often requires engineers to sort through a large amount of information from many different sources, a process that can take months.

A yield manager usually depends on manufacturing process data such as parametric measurements and in-line inspection data when making an analysis. From the performance history of the manufacturing equipment, the yield manager can see which machines have recurring maintenance issues. Electrical scribe-line tests also can provide an early indication that process variations are starting to drift more than expected.

During wafer sort, test sets or patterns generated using ATPG (automatic test pattern generation) software are applied to the die on ATE (automated test equipment). At this point, the yield manager often uses a spreadsheet to plot the cumulative errors from many wafers into a single wafer map that helps identify a failure "signature."

The yield manager then selects a set of die that most likely contain the yield-limiting defect and sends them to the failure-analysis lab for more detailed analysis. The die-selection criterion is often at a very gross resolution, and it's common for many (100 or more) die to be sent for further analysis.

In the failure-analysis lab, the engineers verify the failure for each die on a functional tester to ensure the failure's electrical signature can be duplicated. Then, an engineer attempts to localize the defect to a small block of circuitry and functionally and logically locate the defect in the failing circuit.

Physical fault isolation is the next step the engineers perform, using tools and techniques such as scanning electron microscopes, voltage contrast, and micro- or nano-electrical probing. They physically deprocess the part and then section it to identify the root cause of the yield-limiting defect. Once the cause has been identified, the manufacturer can finally take corrective action, whether it is to change the design, library, or manufacturing process.

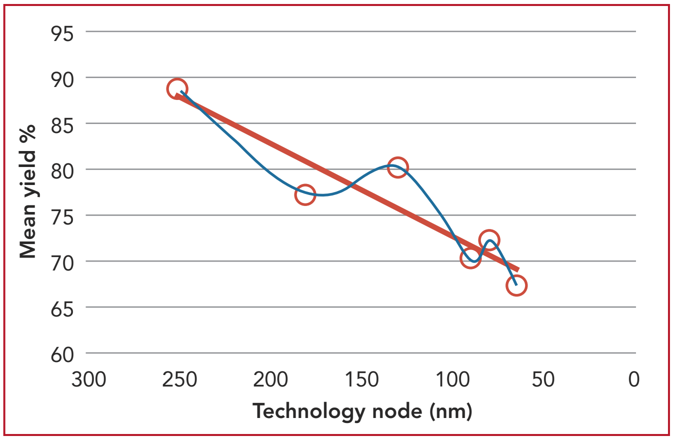


FIGURE 2. Mature yields (that have been in production for as long as 12 to 18 months) decrease an average of 5% for each technology node. Source: Selantek, 2007.

Roadblocks in the yield-management system

For well-characterized processes such as those for feature sizes of 90 nm and greater, designers usually can be sure that their designs will provide acceptable yield when they follow foundry-supplied DRCs (design rule checks). Yield limiters are typically caused by the manufacturing process and are easy to identify, so 90-nm designs tend to ramp to volume quickly. Expected manufacturing variability that may cause defects is taken into account within the DRC.

At designs nodes below 90 nm, however, yield-limiting defects can be design- or feature-related and are harder to identify. Because the manufacturing processes for these designs are not as mature, unexpected interactions between design features and manufacturing variability are causing an increase in yield-limiting defects. And these often appear to be randomly distributed across the wafer and across lots, making it difficult for the yield manager to identify which devices are affected by systematic issues.

In addition, at very small feature sizes, little real margin exists between the design rules and manufacturing process variations, leading to an average 5% decrease in expected yield with each successively smaller design node for mature products that have been in production for as long as 12 to 18 months (**Figure 2**). Optical resolution also has become an issue with smaller feature sizes and more metal layers. It's becoming increasingly difficult to visually identify an issue based on analysis of

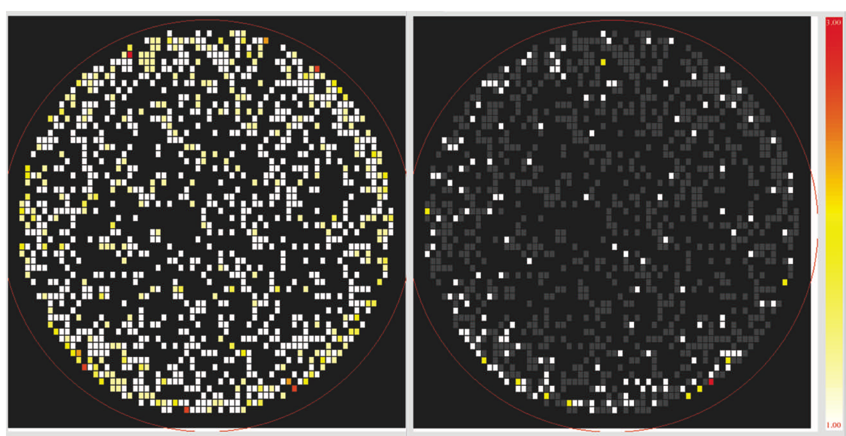


FIGURE 3. A wafer map that shows all failures can hide root causes in the "noise" (left). A map of failing die due to one failure mechanism (right) helps with diagnosis.

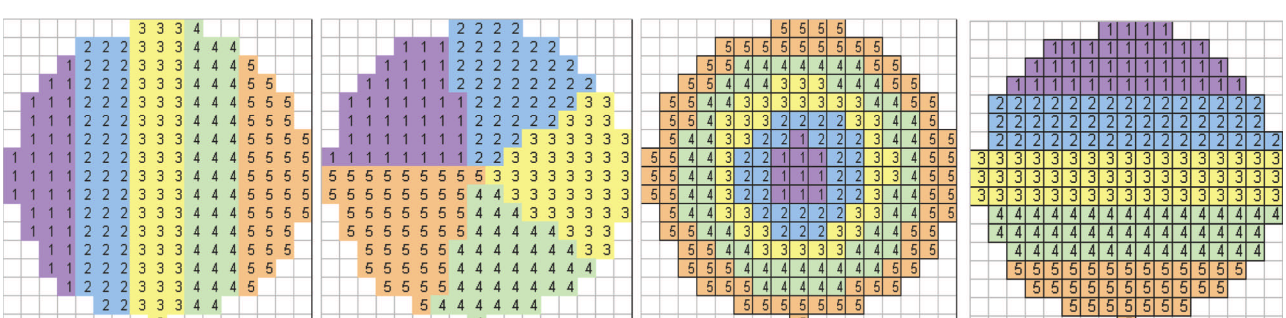


FIGURE 4. A yield-analysis tool can allow yield managers to specify wafer zones for analysis.

test signatures and manufacturing data alone without the netlist.

To complicate things further, the yield manager may not have access to manufacturing equipment data, the results of optical inspection tests, or wafer-position data. In this situation, the manager has to determine the root cause of systematic yield-limiting defects without all of the data that traditionally has been available. The yield-analysis engineers may need additional time, effort, and money to identify and locate defects with this limited data set.

Automated diagnosis provides a better roadmap

One way to improve the time to yield for advanced ICs is by using a diagnosis-driven yield-analysis process that enables the yield manager to make better use of manufacturing test results to find out why and where failures occur. Instead of relying solely on pass/fail information from manufacturing test, the yield manager can take advantage of commercial logic-diagnosis software tools that provide detailed data from the manufacturing test—not just which test pattern failed, but exactly which ones out of millions of cycles failed and for what pins. Engineers can use this detailed information to determine exactly what the defect is and where it occurs. And some vendors provide logic-diagnosis software that is compatible with their on-chip compression software, so the yield manager doesn't have to decipher compressed data (Ref. 1). The manager can have the software generate diagnosis reports for each failed die, which can then be used to group the die based on matching of specific failures, such as bridges, opens, cell, and metal layers.

At Mentor, our logic-diagnosis software can automatically diagnose large amounts of failures after wafer sort at the same time that manufacturing test is running, which means the yield manager doesn't have to wait until test is finished for the data to be available. When a die fails a test, the failure log can be sent immediately to a database that also includes diagnosis results. The yield manager can generate a report for each die that specifies the most likely cause of the failure.

In addition, the logic-diagnosis tools can perform diagnosis based on the design and physical layout data, not just on the manufacturing test set. By incorporating the layout information, the tools determine the type of defect and localize it down to its physical coordinates much more quickly than can be done manually, giving the yield manager a head start on identifying defect types and which pin, cell, net, or group of nets may be causing the test failure.

For logic-diagnosis software to be useful in ramping yield, the yield manager must be able to analyze the diagnosis results and differentiate systematic defects from random ones. The manager can generally accomplish this by performing a statistical analysis after diagnosing a large number of failing devices. For instance, after diagnosing the test failures, the yield

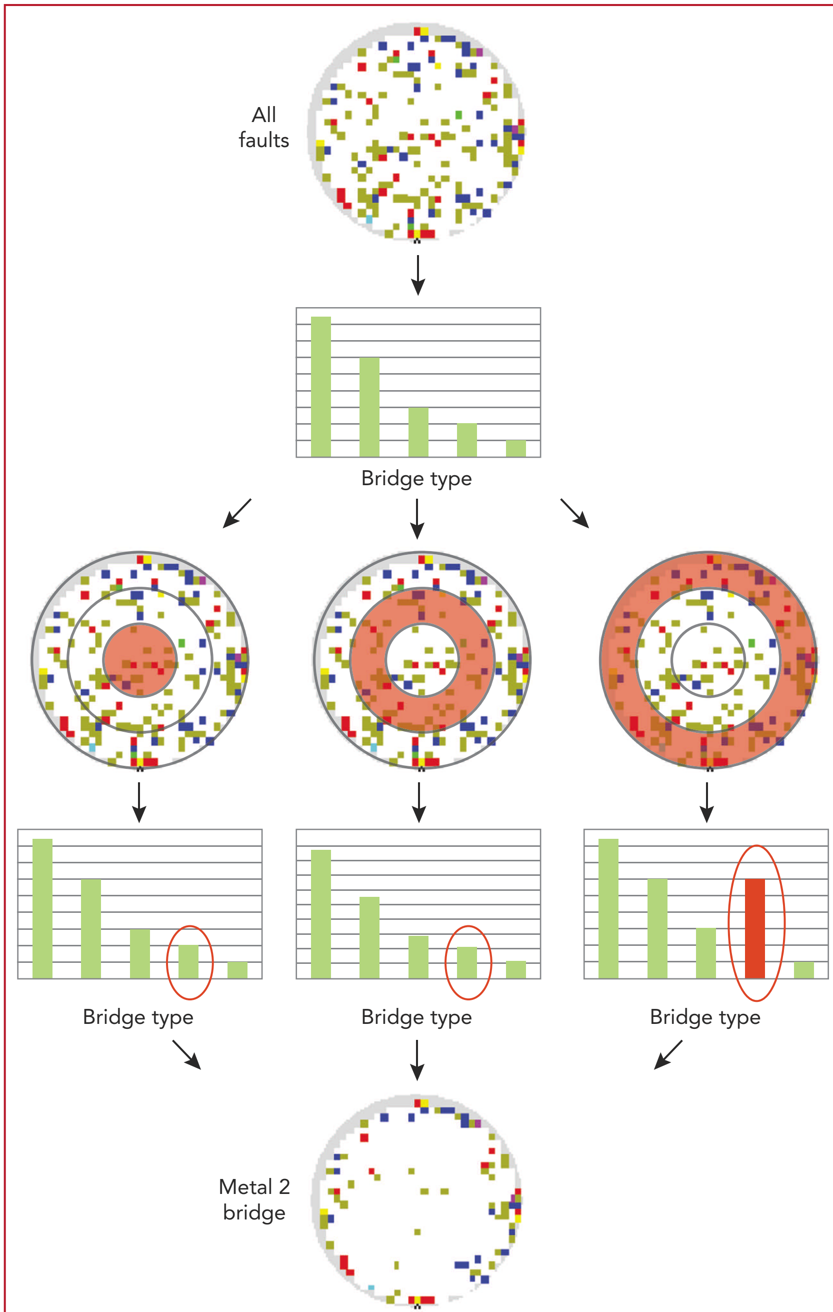


FIGURE 5. With diagnosis-driven yield-analysis tools, manufacturers can analyze a feature type (a bridge, in this example) in a particular zone of a wafer, and the software can then display the failure signatures and instances of a systematic issue.

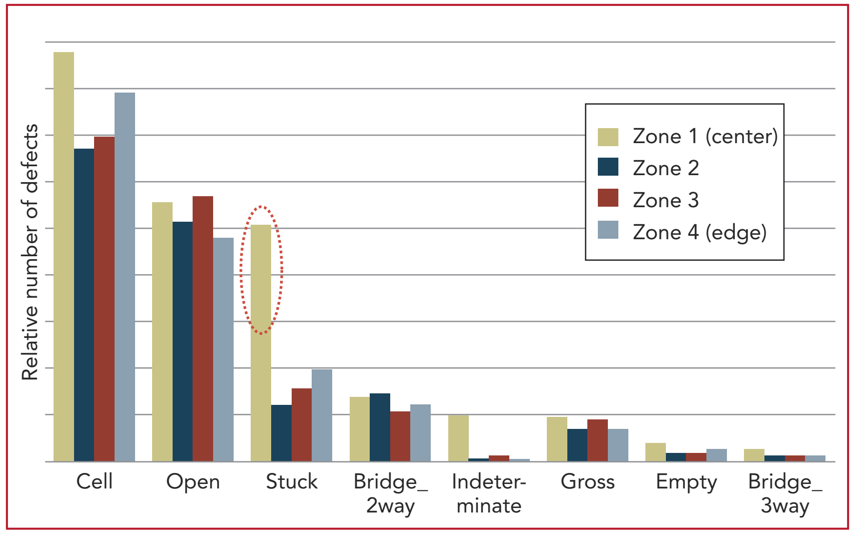


FIGURE 6. A Pareto chart highlights the occurrence of systematic defects per wafer zone.

manager may find that many parts have a bridge defect in the same location. Statistical analysis may help determine that, while several types of defects are randomly distributed across the wafer, this particular defect only occurs in the center of the wafer—indicating a systematic issue. **Figure 3** shows how systematic problems can be extracted from the "noise" in a stacked wafer map.

To make the yield manager's job easier, a yield-analysis methodology that includes statistical analysis that displays different failures mapped across wafers, lots, scan chains, and the die can be used. This methodology allows the yield engineer to see if specific defect mechanisms are evenly distributed, or if there is a correlation with a specific type of defect and a specific part of the die.

Yield-analysis software can indicate a systematic defect as

- the aggregation of a failed feature,
- the difference between the expected and actual failure probability of a failed feature, and
- a group of failed features that is sensitive to certain regions of a stacked wafer map.

With this yield-analysis methodology, the yield manager can analyze a "zone" or area of the wafer (**Figure 4**) for failure characterization. Using this method, a full analysis could be performed without prior selection. Yield-analysis software tools can then automatically analyze the preselected population according to the zone and display the failure signatures and instances of a particular feature failure (**Figure 5**). The features with the highest probability of systematic defects are displayed with a Pareto chart (**Figure 6**). The software then allows the yield manager to drill down into the data and see which die on the wafers match a failure signature.

Failures are categorized in a way familiar to the yield manager, such as by scan chain number, test pattern number, scan cell, net name, metal layer, and diagnosis type. Examples of diagnosis types are cell-internal failure, open, bridge, and slow-to-rise.

The tool then creates and displays a stacked wafer map based on the analysis

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filter selected by the yield manager, whether the results are from one wafer or hundreds of wafers. Systemic failures that occur in a non-evenly distributed fashion across wafer zones become obvious. The die locations that show defects occurring most often within the population are highlighted, so the most likely candidate is even more obvious. Then, the yield manager can produce a report generated by the software that pinpoints the defect's exact location and describes the failure.

Using an automated system to perform these tasks helps the yield manager more accurately narrow down the defect to a small number of die that can be sent to the failure-analysis lab for further investigation. Along with the die, the manager can supply the lab with detailed information about where to look and what to look for to speed up the process of discovering and verifying the root cause of a yield-limiting defect.

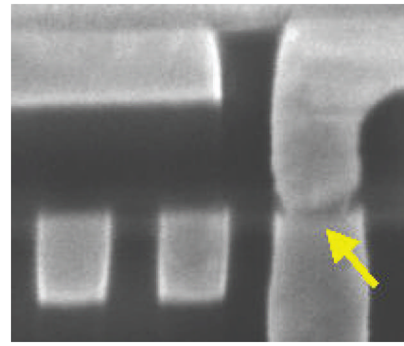

FIGURE 7. The physical-failure-analysis process on eight selected dies isolated a defect to a malformed layer 2 via, which was leading to an open net.

Identifying an open net

Several semiconductor companies were able to benefit from our diagnosis-driven yield-analysis methodology. In one example, a customer had one wafer excursion on a 10-million-gate design at 90 nm. Out of 209 scan fails, diagnosis showed that just over half of the die on the wafer exhibited a defect due to an

open defect mechanism. The customer concluded that the cause of the yield excursion was most likely an abnormality in a process step related to the fabrication of single vias in layer 2.

To validate that conclusion, the customer selected eight failing die and performed detailed physical failure analysis on the defects. These die were selected using diagnosis results from wafer-probe testing. The failure-analysis process on all eight dies isolated the defect to a malformed layer 2 via that was leading to an open net in the device (**Figure 7**). The failure-analysis information can also be used to identify and correct the deviant process step to restore the yield back to normal levels (Ref. 2).

Enhancing yield for a new SOC

In another example, a manufacturer performed a logic diagnosis on 20 scan fails during preproduction, and the results narrowed down the scan chain failures to one suspect that should be either stuck-at-1 or stuck-at-0, a hard defect in silicon. Three devices were sent to the failure-analysis lab with a diagnostic report that indicated the scan input path that was a suspect as well as the scan cell. The results of the physical failure analysis were inconclusive and indicated that the defect could be random or was randomly distributed on the die.

When the manufacturer used the diagnosis-driven yield-analysis flow, however, filtered wafer maps showed that there was a higher percentage of scan chain failures in the edge of the wafer than at the center. The exact fault location in the scan chain failing units was isolated. The failure analysis showed poor copper fill, and the process steps were enhanced for all the metal layers. As a result, the manufacturer reduced scan chain failures from 13% to 3%, increasing the yield by 10%. Using diagnosis and physical failure analysis on what appeared to be randomly distributed chain defects helped improve the total yield (Ref. 3). T&MW

REFERENCES

1. Press, R., "Embedded Compression for Production Test," *Evaluation Engineering*, October 2007. www.evaluationengineering.com.

2. Sharma, M., et al., "Efficiently Managing Yield Excursions by Identifying Physical Root Cause from Test Fail Data," *Proceedings of the 2008 International Test Conference*. www.itctestweek.org.

3. Ponnuvel, G. et al., "An Industrial Case Study of Diagnosing Randomly Distributed Chain Defects for Process and Yield Improvement." Presented at the 5th IEEE International Workshop on Silicon Debug and Diagnosis. www.sdd-online.org.

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34410A	6 ½	0.0030%	10,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34411A/ L4411A	6 ½	0.0030%	50,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34420A	7 ½	0.0030%	250 / sec	.02 sec	GPIB, RS-232
3458A	8 ½	0.0008%	100,000 / sec	3.0 ms	GPIB

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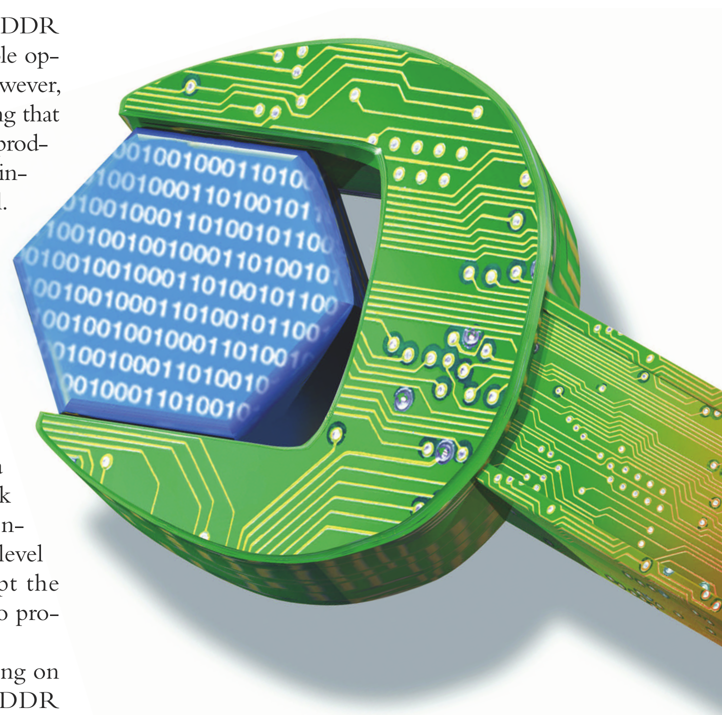
Tune and test DDR MEMORY



Modern electronic devices rely on stable DDR (double data rate) memory for fast, reliable operation. A shortened time to market, however, often limits the amount of product testing that you can perform. Microprocessor-based products released with unstable memory may experience only intermittent failures, but even those can lead to a costly recall. To minimize that risk, you can follow a comprehensive memory tuning and testing process that you can verify with an oscilloscope or logic analyzer.

Tuning is part of configuring a computer system's DDR memory. Device-specific tuning will match a DDR memory device's timing parameters with the configuration registers in the DDR memory controller's CPU. Data sheets for DDR devices specify the timing required for proper operation, listed as fractions of a second. You must convert these timing parameters to clock cycles before you can program them into a memory controller. For this conversion, you should write some high-level DDR memory configuration software that will accept the standard timing data from a data sheet and convert it into processor clocks for low-level DDR memory drivers.

The next step of the tuning process will vary depending on your product's CPU. Many CPUs let the user tune DDR

DOUBLE DATA RATE MEMORY POSES A TRADEOFF BETWEEN PERFORMANCE AND STABILITY.

BY ANDREW FISH, KOZIO

memory parameters such as signal termination and read/write delays that may be specific to a particular board layout. The user manual for a DDR memory controller will specify any tuning capability that it provides.

Read/write delays

When included as part of the DDR memory controller, modified read delays or write delays can lead to the most stable system. A product may have several read/write delay values for which the DDR memory device will work—a window of operability. You should test those delay windows under a range of operating conditions, such as varying temperatures, to find the settings that will optimize DDR memory reliability.

(continued)

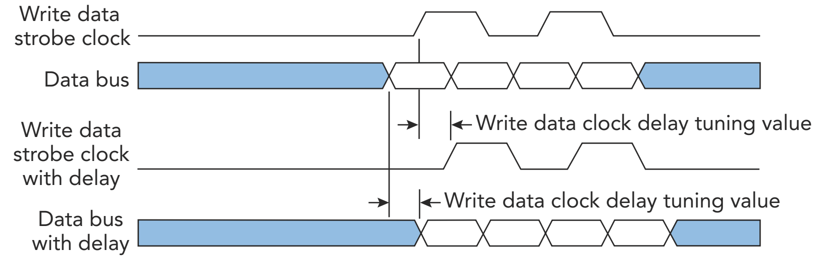


FIGURE 1. Adding delay to a write cycle can improve performance and system stability.

Figure 1 depicts the timing of DDR memory write cycles with and without delays. You may need to add delays because the strobe and data transfer will shift in time relative to the DDR memory clock (not shown in Figure 1). In some cases, the read/write delay tuning and adjustment will occur every time a user powers on the product. Many designs, however, rely on this tuning process to occur during design only, with the released product using the optimal values that balance performance and reliability.

After you complete the initial tuning, you should put the product through several levels of validation testing. In some cases, testing will reveal the need for additional tuning. The key to effective DDR memory testing is to make your tests progressively more difficult, covering connectivity, memory retention, stress, and performance.

A best practice in DDR memory design is to manually verify that the PCB (printed-circuit board) traces are connected. You can use an oscilloscope, logic analyzer, or multimeter for this connection test. Once you complete this initial design check, software tests can verify the DDR memory address and data line connections for proper operation at the speed of the processor. An address bus test writes a base pattern and then a test pattern to all power-of-two offsets (0001h, 0002h, 0004h, etc.). Data bus tests use a "walking-ones-and-zeros" pattern that tests across the width of the data bus on a single memory word. These tests verify that no shorts exist to power or ground or between any data lines or any address lines.

MSB								LSB
0	0	0	0	. . .	0	0	0	1
0	0	0	0	. . .	0	0	1	0
0	0	0	0	. . .	0	1	0	0
				⋱				
1	0	0	0	. . .	0	0	0	0

FIGURE 2. A walking-ones data pattern ensures that no shorts exist across data lines.

Walking ones

For a walking-ones pattern, your software, whether purchased or written in-house, must perform successive writes to the given address. First, the software sets the LSB (least-significant bit) to 1 and all other bits to 0. Next, the software sets the next LSB to 1 and all other bits to 0; and so on, until each bit has been set to 1 (**Figure 2**).

After you verify connectivity, you should run functional validation tests to ensure that all the memory cells in the DDR memory can retain the values written to them. Filling and verifying all the cells with their own address values as data can accomplish this task. Additionally, you should fill all the cells and verify that all the memory cells can store both ones and zeros. Use the one's complement of the cells' addresses to run this test.

Several advanced CPUs include software that performs DDR memory stress tests, which ensure that the memory can perform at your system's full speed. Such processors can simulate an application-like environment. By running your functional tests with cache enabled, you will also force data bursts between the processor and DDR memory as cache lines get flushed and replaced. Running DMA (direct-memory access) loop tests while also receiving Ethernet packets via interrupts can cause multiple simultaneous DDR memory reads and writes that will stress the memory and ensure coherency.

Figure 3 illustrates the block-level interaction of the DDR memory with a system's cache memory, DMA, and Ethernet controllers. Each line between the components represents data transfers from one logic component to the other. In the case of DMA, you can program multiple transfers to occur simultaneously across multiple channels. The actual number of channels is a feature of a particular microprocessor.

Knowing that your DDR memory is properly connected and won't produce errors under stress isn't always enough. You must also measure how well the DDR memory performs. Using a software test with optimized read and write routines, you can determine whether the performance and throughput of the DDR memory are fast enough to ensure that software running in your system will run properly. You must measure performance early in a product's development to resolve any bottlenecks in the data path.

Dedicated applications

When developing software for tuning and testing DDR memory, you should implement the needed routines in a dedicated software application. Although you could develop JTAG tests for tuning and testing—a fairly simple process—you wouldn't be able to operate the DDR memory at a processor's full speed, which is a major testing limitation. Building DDR memory tests on top of an application is also a tempting option, but this approach for memory testing makes it difficult to find a problem's root cause because of the many layers of software that test routines use.

You should develop modular DDR memory test software (**Figure 4**) so you can reuse test routines across departments throughout your organization. Design engineers can use the software for initial

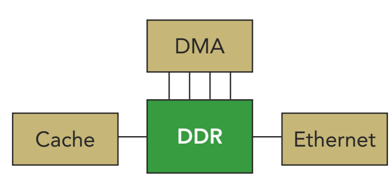


FIGURE 3. During a test, DDR memory must interact with cache memory, DMA, and Ethernet controllers.

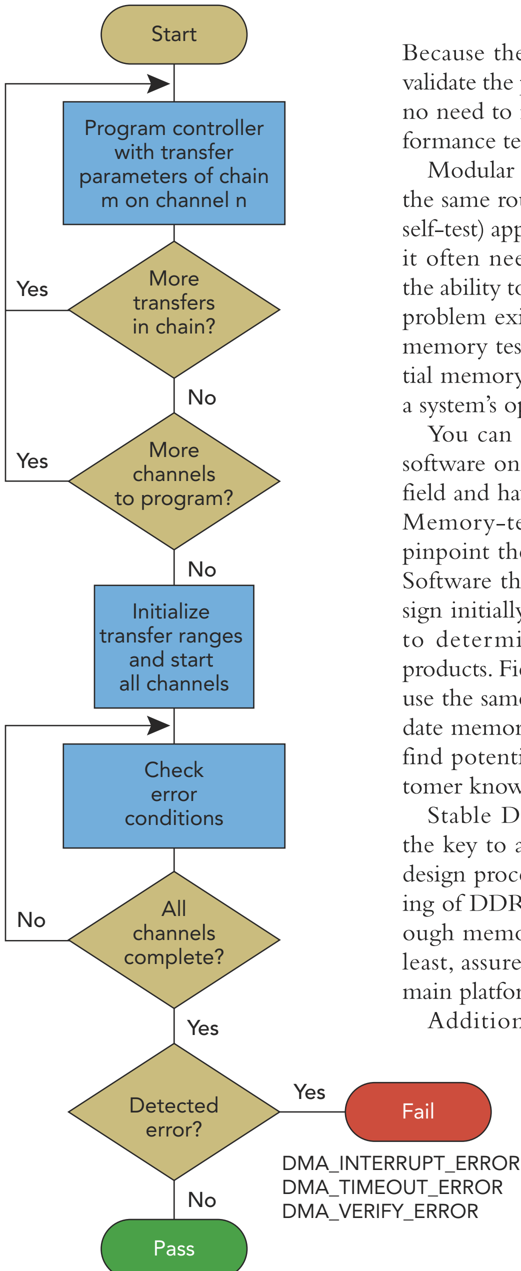


FIGURE 4. Modular test software lets engineers share test routines across departments.

board verification. Test engineers can use the test routines to determine if a problem is related to hardware or software by using known-good tests. A known-good test contains no programming errors that would produce false results, such as identifying errors that don't exist or missing errors that do exist.

Test engineers and manufacturing engineers can also use the test routines to verify data paths and general functionality. Because the same software was used to validate the product's design, there will be no need to rerun extensive stress or performance tests during manufacturing.

Modular software will also let you run the same routines in a POST (power-on self-test) application. If POST is required, it often needs to run quickly but have the ability to warn end users if a memory problem exists. Thus, you can use DDR memory test routines to uncover potential memory problems before they affect a system's operation.

You can also use DDR memory test software on units that have failed in the field and have been returned for service. Memory-testing software can quickly pinpoint the root cause of the problem. Software that effectively validates a design initially should always be sufficient to determine problems on returned products. Field application engineers can use the same set of software tests to validate memory during customer visits and find potential problems before the customer knows that a problem exists.

Stable DDR memory can often be the key to a company's success. Using a design process that includes proper tuning of DDR memory, followed by thorough memory validation testing will, at least, assure you that you have a stable main platform.

Additionally, if you create a DDR memory tuning and testing process using a modular software approach, you can reuse the process throughout your organization. Not only will the reuse save money, it will help your company to build reliable products and correct memory faults—whether found during development, in production, or in the field. Stable memory can't guarantee that your product will be a success, but neglecting to spend time ensuring that your product has stable memory will nearly always lead to failure. T&MW

***Andrew Fish** is a senior contributor to Kozio's library-based functional tests. He joined Kozio in 2004 and has more than 11 years of embedded programming experience. Fish has developed advanced test capabilities and support for numerous microprocessors and peripheral technologies. He holds a BSEE from Marquette University.*

Testing E-OTD

An emulation-based approach can test 3GPP Enhanced Observable Time Difference capability in GSM/ GPRS and W-CDMA handsets.

BY DARCY SMITH, AGILENT TECHNOLOGIES

To ensure that the 3GPP's E-OTD (Enhanced Observable Time Difference) capability found in today's GSM/ GPRS and W-CDMA mobile handsets operates as anticipated, you need to test the handset's performance. The simplest way to do that is to emulate only two cell towers with a known, but fixed, offset in timing between them. This approach could serve as a quick check, but it falls far short of a real characterization.

For a detailed characterization of E-OTD operation, manufacturers must emulate multiple cell towers, mobility, and variable channel conditions (see "Location-relevant information and E-OTD," p. 51). One plausible means of accomplishing a thorough characterization is through the use of a test system that emulates 12 cell towers with independent time-delay elements and variable channel conditions. As part of the test setup, a channel simulator, often called a fader, provides the time delay from the cell to a phone as well as the fading channel conditions. Just as a real network must calibrate the actual system time, the test system must calibrate the timing of each cell emulator, including both the timing from frame-to-frame and the offset in frame numbers from cell-to-cell.

Using such a test system, you can easily perform tests for a stationary handset. You can hypothetically place the cell towers at known locations on an x-y grid, representing longitude and latitude, and you can place the handset, either deterministically or randomly, at some spot on the grid. The test system computes the propagation delay from each cell tower to the handset location and enters it into the delay elements of the channel simulator from each cell. In this way, the arrival times at the handset are delayed as if in a real system. The handset makes its

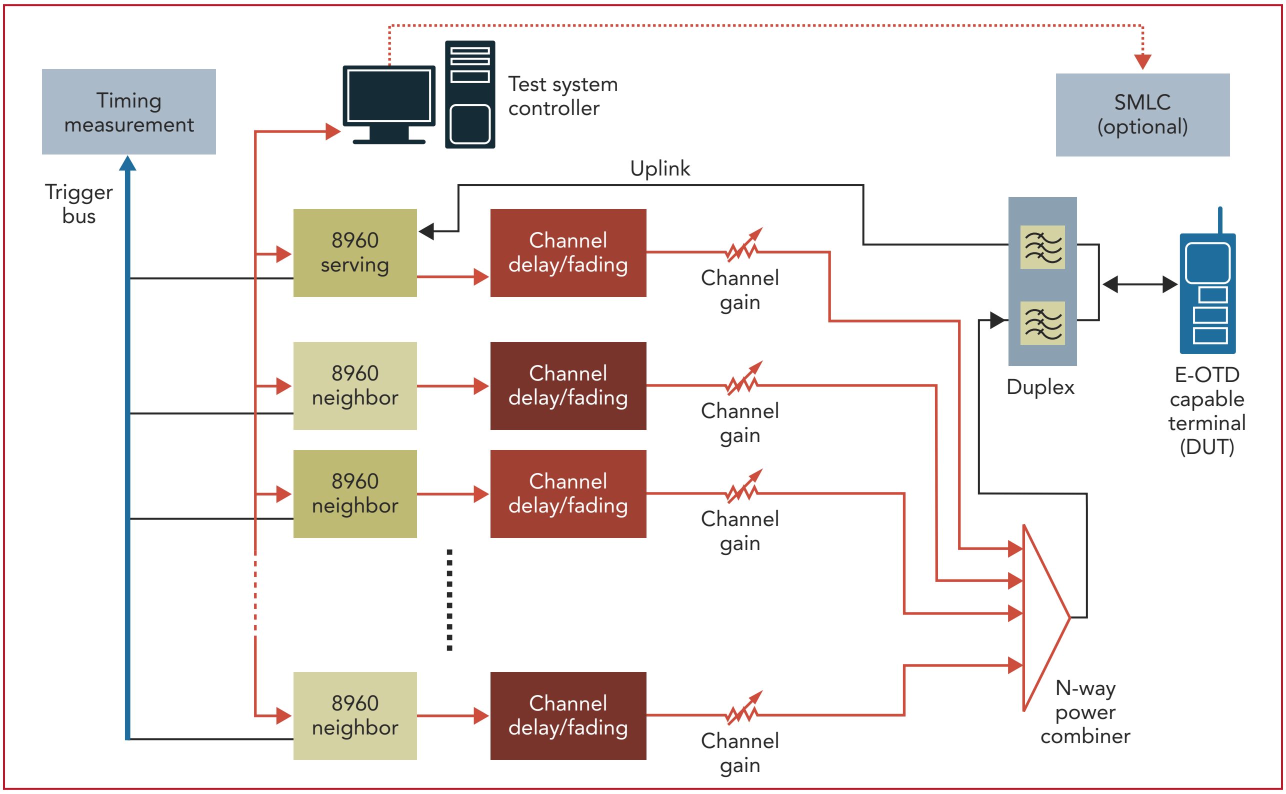


FIGURE 1. In this test system configuration, an 8960 wireless communication test set serves as the emulator for individual base stations; a channel simulator mimics channel delay and fading. The test set can be used as the serving cell in an E-OTD test system to issue location requests to a mobile handset and then receive location estimates or measurement results in response.

E-OTD measurements and computes its location by using the data from the handset and the system calibration values. You can then verify the results against the location of the handset on the grid. Alternatively, in assisted mode, the mobile handset reports the timing measurements back to a network entity called the SMLC (Serving Mobile Location Center), which in turn uses them to determine the handset's location.

To create variations in this stationary test scenario, you can change the settings for variables such as the amplitude from each cell, the channel fading from each cell, and the interference from distant cells (on any of the measurement channels).

For a typical nonstationary test scenario, you can emulate the slow movement of the handset in the network by changing the time delay and signal levels from the different cell towers. As cells fall behind the coverage path of the handset, they are reassigned ahead of the handset's path with new x and y coordinates and are slowly brought back into the handset's range.

In either the stationary or nonstationary scenario, the control interface between the cell tower and handset for E-OTD control and measurements is generally carried on a message similar to an SMS (short message service). The cell uses a downlink message to command the handset to make an E-OTD measurement. The results are then reported on the uplink using these special SMS messages.

To accommodate various use scenarios and requirements, you can configure a cellular system simulator by using 12 base-station emulators (**Figure 1**) configured for either GSM/GPRS or W-CDMA operation. You can simulate changes in the position of the mobile handset by varying the delay from each cell tower to the handset. This delay is controlled by the time delay in a channel simulator.

Calibrating the W-CDMA test system

Testing the E-OTD capability in a W-CDMA handset can be especially challenging, due to the difficulty in finding the relative frame numbers and frame-time offset. To better understand how to deal with this challenge, consider a transmission from three hypothetical cells and the BCH (broadcast channel) framing. The BCH—a logical channel that is 20 ms in length and carried on two consecutive physical frames—contains the frame count parameter used in E-OTD along with the time of arrival of the frame start.

In **Figure 2**, the top diagram shows the relative timing near frame 0 from cell 1. Here, you must determine the values for x and y (integer frame offsets) and the delta between the start of the frame between cell 0 and the other two cells. This delta time must have precision in the tens of nanoseconds.

In W-CDMA, the frames are counted from 0 to 4095 (12 bits). Because the BCH requires two frames to transmit a signal, the value of the frame counter increments by two and contains only even values. In fact, the LSB (least significant bit) is not transmitted, only the upper 11 bits. The real frame count, at the starting frame of the BCH, is calculated by multiplying 2 by this 11-bit number.

Also in Figure 2, the bottom diagram depicts a hypothetical frame timing of the same three cells. The graphic shows the offsets in the 0 frame for the three cells.

In this example, the accurate calibration requires:

- 50-ns (maximum) uncertainty per cell tower. This assumes the worst-case addition of errors to yield 100-ns uncertainty in a single difference measurement.
- 20-ns per cell frame-to-frame timing. The offset of the frame number must be exact; an error in this value equates to a 10-ms offset, which is unacceptable.

Real-world example

You can develop an E-OTD test setup with commercially available instruments, such as the Agilent 8960 wireless communications test set. Using the 8960, you can generate a trigger signal that is synchronized to the frame counter and is at a constant offset from the frame clock. If you use separate test sets to emulate the serving cell and a neighbor cell, you can measure the time interval between the trigger of the two cells to determine the integer and the fractional delay between them.

The difference in frame numbers is given by integer multiples of 10 ms in offset, which represents the difference in frame-to-frame timing, assuming constant timing between the frame rollover trigger signal and transitions in the RF modulation. Generally speaking, the time-delay measurement has these requirements:

- The input must consist of 12 separate TTL signals for a system emulating 12 towers.
- One of the TTL signals (always the same one) must be used as a start timer for all measurements. Each of the other 11 can be considered a stop for its own timer.
- W-CDMA triggers must consist of a single pulse occurring approximately every 42 s. If the 8960 test sets have been turned on at random times, the timing can be considered random across all 12

Location-relevant information and E-OTD

Position-location technology has become an integral part of GSM/GPRS and W-CDMA mobile handsets. Initially, this technology was driven by emergency services initiatives like E-911 in the US and E112 in Europe. More recently, its demand is being driven by commercially available location-based services that provide a handset user with information about traffic, weather, or other location-relevant conditions or activities. Tracking of assets and people as well as location-based or location-sensitive advertising and marketing are two other compelling application areas.

Key to delivering high-value content to a mobile handset is the ability to ascertain the handset's location. To meet this need, the 3GPP's E-OTD (Enhanced Observable Time Difference) position-location technology is being integrated in GSM/GPRS and W-CDMA handsets. With E-OTD technology, the mobile handset essentially triangulates its position using signals from cell towers and then reports that position back to the network.

The E-OTD positioning mechanism, which is described in 3GPP TS 03.71, requires a handset to measure the difference in the time of arrival of signals from several (three or more) cell towers. The E-OTD capability has two basic modes of operation. In handset mode, the mobile handset uses timing measurements to deduce its current location. In assisted mode, the mobile handset reports the timing measurements back to a network entity called the SMLC (Serving Mobile Location Center), which in turn uses them to determine the handset's location.

Radio timing information is typically expressed as a series of measurements, made at the phone, of the timing difference between sets of two cell towers. The handset makes successive timing measurements by comparing timing for one designated cell tower (which acts as the serving tower) against neighboring cell towers.

Each measurement includes two elements: A time difference from cell-to-cell and a frame number. The frame number allows the E-OTD computation to decide whether to adjust the offset measurement by a frame if the original measurement has been made on different frames from the two cell towers. The time difference and the frame number are combined with the precise transmit times and frame numbers of each cell tower to determine the time difference caused only by propagation-time differences to the handset.

The locus of points described by a time difference from two cell towers of known location is a hyperbola. Adding a second time difference measurement based on a third tower enables the derivation of a second hyperbola. The crossing point of these two hyperbolas is the mobile handset's location. But because two hyperbolas usually will cross at two locations, you may need a third difference measurement, involving a fourth cell tower, in order to guarantee the computation of a unique location for the handset.

A real system can generate the transmit timing information in several ways. One way is through the use of an LMU (location measurement unit) that is capable of making precise timing measurements of transmit time relative to a common clock, typically the GPS. Alternative configurations include one LMU at each cell tower or one LMU at a known location with good propagation characteristics (for example, line of sight) to all the cell towers being calibrated. Using any of these configurations, the LMU can make the necessary difference measurements, as well as derive the time offsets that match its location. Note that the LMU can simply be a mobile station with measurement capabilities.—*Darcy Smith*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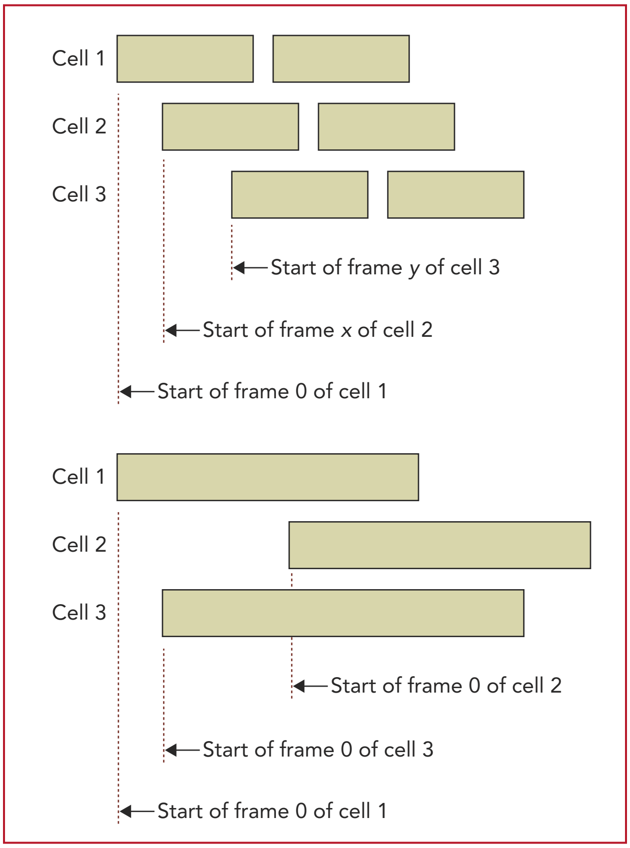


FIGURE 2. The top diagram depicts the relative time of three hypothetical cells, while the bottom diagram shows the corresponding hypothetical frame timing.

units. Consequently, there can be as much as a 42-s delay after the system is armed before the start trigger occurs and up to another 42-s delay before the last unit sends its stop trigger.

- You must configure the trigger out of unit 1 to start a time-interval measurement, and you must configure the triggers out of the other units to be stop interval triggers.
- The test-time range needs to go up to 42 s, with a resolution and accuracy of approximately 1 ns, requiring 11 digits and a long measurement period.

The test process outlined in "E-OTD test steps" (p. 54) speeds up the test process, forcing all measurements to occur within a 10-s window (the entire test takes about 50 s) and dropping the timing resolution requirements to 10 digits. As a tradeoff, however, all frame count numbers must be in close alignment.

The timing measurement for GSM handsets is similar to that for the W-CDMA process, but the GPIB command for GSM sets the counter approximately 1 s before its frame rollover. This eliminates the delay in step 5 of the test process. Also, it establishes the initiator as a dedicated frame-reset command on GPIB to test test set 1 in step 1 and to test the rest of the test sets in step 3.

With the market for location-based services continuing to grow, technologies like the 3GPP's E-OTD have become increasingly important. Being able to adequately test this position-location capability in GSM/GPRS and W-CDMA handsets is equally important and requires a test system capable of

E-OTD test steps

This seven-step process completes all measurements on an E-OTD handset within a 10-s window.

1. Reset the frame counter to zero at some unknown time after sending a format-change command (for example, "Cell 1 to W-CDMA"). The time duration for the reset is 0 to 1 s. (The system requires a full timing reset even if the format doesn't change.)

2. Wait 0.2 s. Adding this small delay ensures that the trigger from test set 1 will always lead the triggers from the other test sets.

3. Reset the format of all other cells, either through a group-execute function or in a quick sequence.

4. Set the frame-rollover triggers, enabling the trigger out from each test set.

5. Wait 39 s. Note that the delay from frame 0 to the trigger out of each test set is 40.96 s.

6. Arm the time-interval measurement. The trigger from test set 1 (start timing measurement) should occur in approximately 1 s.

7. Collect the results. The trigger out of the rest of the test sets should follow that of the first by about 0.2 s. These are the stop measurement triggers.

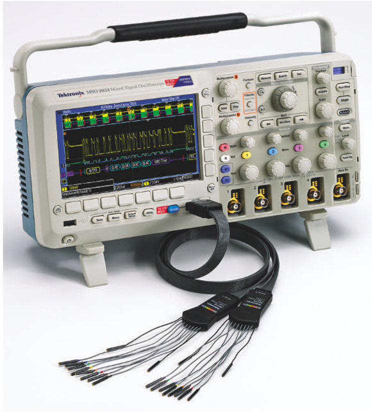
making accurate radio timing measurements. The test system I have proposed offers a plausible means of accomplishing that goal and, as a result, can play a key role in ensuring that E-OTD-enabled GSM/GPRS and W-CDMA handsets perform as expected. T&MW

Darcy Smith *is a product marketing and applications engineer for Agilent Technologies' Mobile Broadband Division. She is currently responsible for W-CDMA/HSPA One Box test products for the R&D market. She graduated from the University of Washington in 1997 with a master's degree in electrical engineering. She also holds a bachelor's degree in business administration from Washington State University.*

MSOs focus on serial buses

The MSO2000 series of mixed-signal oscilloscopes from Tektronix can trigger on and decode low-speed serial buses such as I²C, SPI, RS-232, CAN, and LIN using their analog channels. The MSOs also provide 16 logic inputs for testing parallel buses and I/O lines.

Available in 100-MHz and 200-MHz models with two or four analog channels, the MSO2000 series incorporates Tek's Wave Inspector, which lets you scan a captured waveform and zoom in on details. Wave Inspector lets you "bookmark" points in a waveform and tells you how many triggers occur in a 1-Msample captured waveform.



The MSO2000 also adds FilterVu, a digital variable low-pass filter that lets you reduce unwanted noise from a signal. Reducing noise can reduce false triggers, especially when using edge triggering.

Serial-bus decode eliminates the need to manually count bits and find characters transmitted on the bus. As you expand a captured waveform to see individual bits, the MSO2000 will determine the bits and frame them for easier reading.

Base price: $3580 for two 100-MHz analog channels and 16 logic channels. *Tektronix, www.tektronix.com.*

V6000 tests both flash and DRAM

Verigy has announced the V6000 for testing both flash and DRAM memory on the same automated test equipment platform. The V6000 family of testers includes the V6000e, which supports memory test-program development and device characterization in the office or lab environment; the V6000 WS, which enables 300-mm one-touchdown wafer-sort probing for both flash and DRAM applications; and the V6000 FT, which performs single-insertion final test of flash, DRAM, or MCPs (multichip packages) that include both flash and DRAM memory.

All V6000 systems include Verigy's Active Matrix technology and sixth-generation tester-per-site architecture. The Active Matrix technology provides massive parallelism, supporting more than 18,000 I/O pins and more than 4000 programmable power supplies, and it enhances signal integrity due to shortened signal paths to a V6000 system's pin electronics. The V6000 offers scalable AC performance at 140, 280, 560, and up to 880 Mbps.

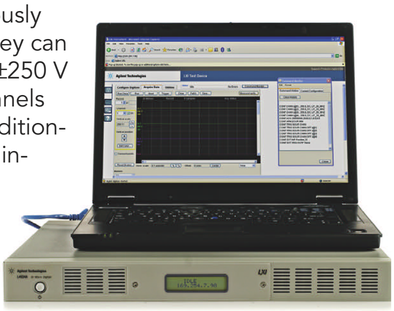
The V6000 can test either flash or DRAM memory by simply changing to a new test program and probe card. Users can upgrade the system performance and pin count by adding test-site modules or Active Matrix modules. The V6000 WS uses low-cost, connectorless probe cards, accommodates different sized probe cards (450 mm or 560 mm), and interfaces to all major probers.

All the V6000 testers also share the same operating system software, hardware, and interface, allowing users to develop, share, and move test programs between testers as devices go from engineering and characterization to wafer sort and final test. With minor modifications, test programs from Verigy's V5000 family of testers can be used with the V6000 platform. The V6000 is water-cooled, requiring a smaller footprint and using less energy than air-cooled systems.

Verigy, www.verigy.com.

Digitizers target auto/aero test

Agilent's L4532A (two-channel) and L4534A (four-channel) digitizers sample at 20 Msamples/s with 16-bit resolution. Aimed at automotive, aerospace, and medical test, the instruments are LXI Class C compliant and include a Web server for control with a browser.



The digitizers simultaneously sample all channels, and they can measure from ±250 mV to ±250 V on their isolated input channels without external signal conditioning. Built-in measurements include minimum, maximum, average, and RMS voltage, rise and fall time, overshoot, frequency, pulse width, and duty cycle.

The L4532A and L4534A's communications ports include GigE (Gigabit Ethernet) and USB 2.0. You can control the instruments through custom applications or through a Web browser when communicating through the Ethernet port. A command-monitor window lets you see the SCPI commands that correspond to browser actions, such as "setup" and "acquire data." You can paste

> > > > > > >

those commands into custom software for the instrument.

Prices: L4532A (two channel)—$6500; L4534A (four channel)—$8500. Each comes with 32 Msamples of acquisition memory; an upgrade to 128 Msamples adds $1500 to both prices. *Agilent Technologies, www.agilent.com.*

Interface converts RS-232 to USB

The OM-CONV-USB interface converter from Omega Engineering includes driver software and has a data transfer rate of greater than 1 Mbps. The product is powered from the USB cable, so no external power is required. A user can install the driver software into the PC and connect the converter into the PC's USB port; the PC will immediately recognize the device. Then, the user can connect the converter to a serial device such as a modem, serial printer, or instrument.

Base price: $15. *Omega Engineering, www.omega.com.*

JTAG Technologies debuts boundary-scan I/O module

The compact JT 2149/MPV DIOS (digital I/O scan) module provides test access to printed-circuit boards requiring external I/O stimulus and response monitoring.

The MPV (multi-programmable/multi-voltage) DIOS plugs directly into JTAG Technologies' QuadPOD, the standard front-end of the DataBlaster series of boundary-scan JTAG controllers. When connected to a circuit board via edge connector or fixture test pins, the module exercises the board's connections in synchronization with the boundary-scan infrastructure. The DIOS module supports the vendor's new SCIL (Scan Configurable Interface Logic) technology to allow custom functions such as pattern generators, counters, and bus simulators to be factory formatted for advanced functional and pattern-oriented testing. SCIL supports at-functional-speed testing of non-boundary-scan logic clusters, which can also be tested using static patterns.

While the module occupies one of the TAP locations in the QuadPOD, the system still provides four independent TAPs to the unit under test by means of a stream-through function. The DIOS module is backward compatible with other JTAG I/O scan systems, and both output and input thresholds can be programmed.

The I/O channels are grouped into blocks of 16 channels. Selected channels can be interfaced with custom cabling to the board under test for low-volume applications or interfaced with bed-of-nails fixtures for higher volume production. The I/O channels are individually programmable as input, output, bidirectional, or tristate signals.

Price: $1250. *JTAG Technologies, www.jtag.com.*

Test & MEASUREMENT WORLD

Line-scan cameras adjust to low and variable speeds

By Ann R. Thryft, Contributing Technical Editor

When building an inspection system for low-end PCBs (printed-circuit-boards), you can obtain high-resolution images for less cost by using line-scan cameras instead of area cameras. But it has been difficult for line-scan cameras to achieve high resolution and good image quality while the object being imaged is moving at very slow or variable speeds.

Basler Vision Technologies' product manager Henning Tiarks described the challenges of slower and variable speeds and how these can be overcome by designing sensors and camera electronics together.

Q: Why do line-scan cameras have difficulty adapting to slower and variable speeds?

A: In inspection systems that use line-scan cameras, these cameras are positioned above PCBs that move continuously underneath, while they scan boards line by line to build an image. The cameras must be synched with the boards, which in the past demanded constant board speeds. Slower speeds are used mostly for low-cost systems that inspect PCBs targeted at low-cost markets.

High performance at low speeds is challenging for line-scan cameras because low speeds can mean long exposure times. Although longer exposure times can provide more detail, they also mean a greater chance of artifacts—created by light in combination with noise from the camera's electronics—that degrade image quality. One way to solve this is to make the sensor quickly dump the electrical charge inside pixels in between each line.

Q: How does jointly designing sensor and camera electronics help this situation?

A: To make the sensor perform a fast dump requires a low electrical charge so it can be dumped in time for the next image. This requires designing the sensor and the camera electronics together, as Basler has done in its runner camera series.

We cover the sensor and measure the noise in the image, so there is no influence of light noise from the sensor, only the influence of electronics noise from the camera. The sensor's frequency varies with variations in heat, as do the frequencies of the camera electronics. If the frequencies inside the camera are dominant, this can create artifacts that can be detected when doing a fast Fourier transformation.

A good design that works in variable heat conditions is therefore essential. This includes taking care of heat dissipation and monitoring temperature inside the camera, as well as choosing electrical components that work stably under different heat conditions. The result is a slowest speed in the runner series of 1 Hz, or 1 line/s, and a fastest speed of 56 kHz, or 56,000 lines/s. Previously, the minimum speed in Basler's line-scan cameras was 1 kHz, or 1000 lines/s.

Q: What else can be done to improve image quality at slow speeds?

A: In low-noise situations, although a higher bit depth digitizes artifacts as well as image data, proportionately fewer bits are affected, so there is more usable information with fewer artifacts. Most line-scan cameras are 10-bit, but we put two more bits in the 12-bit runner series. This increases gray values from 1024 to 4096, giving greater accuracy and a more finely tuned image. □

Henning Tiarks
Product manager
Basler Vision Technologies

INSIDE THIS REPORT

EDITOR'S NOTE

Seeing more, smaller, and faster

By Ann R. Thryft, Contributing Technical Editor

Much of the demand for higher resolution machine-vision tools is coming from the need to see more at a time, more clearly, and at much smaller dimensions than ever before. The semiconductor industry's shift to shrinking process design rules of 55 nm, 45 nm, and below is putting pressure on tool, camera, and microscope makers to improve both resolution and throughput speed.

Several new technologies have been harnessed to address these challenges. One is Carl Zeiss SMT's helium ion source for advanced microscopy that can see greater detail with a smaller focus spot and very little blurring at subnanometer resolutions (see "Helium ion beams illuminate tiny particles" at www.tmworld.com/zeiss_1208). Another innovation is Nikon Instruments' advanced optics that use scattered light and diffracted light for whole-wafer surface inspection, combined with polarized light for pattern detection (see "Polarized optics illuminate wafer defects," at www.tmworld.com/nikon_1208).

At the same time, manufacturers need to inspect larger surface areas, including flat-panel displays, whole wafers, and photovoltaic cells. This means much larger images, and thus more memory, which affects machine-vision software. Many third-party packages now support 64-bit processors with a wider addressable memory (see "Machine-vision software goes independent," p. 64). □

Contact Ann Thryft at ann@tmworld.com.

HIGHLIGHTS

Cameras, motorized lenses, and software debut at Vision 2008

During Vision 2008 (November 4–6, Stuttgart, Germany), numerous vendors introduced products for electronics inspection. **MVTec Software** announced version 9.0 of its Halcon software. Version 9.0 offers improved speeds via Halcon's automatic operator parallelization, which distributes processing to the number of available cores. **Basler Vision Technologies** expanded its product portfolio by announcing the Aviator camera series with two models based on Kodak's KAI-01050 CCD sensor.

To support applications in which a camera must automatically adjust to different sizes, **Leutron Vision** has added a motorized-lens option to its PicSight modular cameras. Cameras sporting the option can connect to motorized lenses with C or CS mountings.

By introducing the VCSBC4012 camera, **Vision Components** extended its VC BoardCam range of intelligent board cameras without a housing. In support of contour-based object recognition, the company highlighted VC Smart Finder software, which allows users to identify structures by means of preset patterns. Also on display was the VC4467 EXview, which features an EXview HAD CCD sensor from Sony that enables the camera to analyze even long wavelength light near the infrared spectrum. The company also announced it has adapted the OpenCV open-source program library to its proprietary VCRT operating system, implementing it on all VC smart cameras.

Dalsa introduced its Spyder3 color camera and two new Genie GigE Vision-compliant cameras—the C1600 and the M1600. **Pleora Technologies** said that eBUS Driver Suite and PureGEV Suite software are now available for all GigE Vision-compatible products, including cameras not based on the company's iPORT IP Engines.

Matrox Imaging debuted the Iris GT smart camera and the Solios eV-CL and Solios eM-CL Camera Link frame grabbers. Designed for harsh, environments, the Iris GT is powered by an Intel 1.6-GHz Atom processor and runs Microsoft's Windows CE 6.0 real-time embedded operating system.

Thermal-imaging system gets upgrade

Used for semiconductor failure analysis, the latest version of the Micro thermal-imaging system from OptoTherm offers a new thermal-imaging camera with a 20-μm/pixel fixed-focus lens, a wide-angle 50° focusable lens, and a 320x240-element uncooled detector. OptoTherm says you can use the Micro system to detect hot spots and shorts, troubleshoot bad components and boards, measure junction temperature, identify die bonding defects, and measure package die thermal resistance.

Micro can measure and display the temperature distribution over the surface of semiconductor devices, enabling quick detection of hot areas that can lead to early failure. The system captures 30 images/s and has a temperature measurement range of 0 to 300°C (32°F to 572°F). Its microscopic lens provides sensitivity of 0.2°C, while the wide-angle lens boasts a sensitivity of 0.05°C. Camera Link and USB interfaces are also provided. www.optotherm.com.

Controllers orchestrate vision systems

Using only two universal control modules, LMI Technologies' Maestro system simplifies the task of connecting the various components of a machine-vision system. LMI says the system is compatible with all cameras and light sources, as well as all machine-vision-software libraries.

A Maestro configuration comprises the P800 master controller and the C12 camera and light controller. The

USB 2.0 cameras target small systems

By Ann R. Thryft, Contributing Technical Editor

Machine-vision cameras with USB 2.0 interfaces are on the rise, as evidenced by recent product introductions from vendors such as Edmund Optics, The Imaging Source, and Matrox Imaging. One vendor that recently entered the USB 2.0 market is Point Grey Research, a company known for its IEEE 1394b (FireWire) cameras.

Vladimir Tucakov, Point Grey's director of sales and marketing, explained the benefits of the new product line. "The USB interface makes integrating the camera with the PC a lot easier," he said. "You can connect a camera to virtually any computer system without adding an interface card. Not all PCs built today have 100-Mbytes/s 1394b ports, but nearly every laptop, desktop, and embedded PC has at least one high-speed USB 2.0 port, with a maximum data rate of 60 Mbytes/s."

When an inspection application calls for resolutions and frame rates that do not require data rates above 40 Mbytes/s (such as 1296x964 at 15 fps), then the USB bandwidth is perfectly appropriate, said Tucakov. Cameras with a USB interface are also ideal for situations that call for low-cost, compact cameras. By employing the USB interface as opposed to GigE Vision, for example, vendors can produce smaller, less-expensive cameras: The USB connector itself is much smaller than many other connectors, and low-cost components like USB cables and hubs are widely available.

Tucakov explained that USB cameras are especially useful in the offline inspection of wafers or circuit boards, where there is less need for high throughput and long cable lengths. He said that smaller USB 2.0 cameras aimed at OEMs, such as members of Point Grey Research's Chameleon family (see **picture**) that measure only 25.5x41x44 mm, can be included as components in small machine-vision systems. "This combination of size and connectivity is important for smaller systems," he said.

Larger, inline AOI machines often contain a complete PC. "But if you are building an offline test and measurement station, containing optics, lighting, camera, and a motion stage," Tucakov said, "you may not want to include an entire PC, since that raises your BOM [bill of materials] by $500. Instead, you can just plug a USB connector into a customer's existing desktop PC or laptop." □

P800 module interfaces with the encoders and the I/O, delivering microsecond synchronization over CAT5e cables for up to eight cameras and light sources, all from a single power supply. All timing, triggering synchronization, sorting, and reject activations are completed by the P800 module.

Devices are slaves to the P800, including the host computer that performs image processing. Camera image data is delivered directly to the computer over standard interfaces, such as GigE Vision or IEEE 1349, with all timing dictated by the P800 and communicated to the computer over Gigabit Ethernet.

The C12 camera and light controller powers and triggers any camera and also provides synchronized high-current pulses for LEDs or lasers.

You can configure a Maestro system with TCP/IP and XML or with a Web-based browser. You can also integrate LMI's FireSync, Sensors that See, and Hexsight components with standard camera and lighting components. www.lmitechnologies.com.

Machine-vision software goes independent

By Ann R. Thryft, Contributing Technical Editor

A growing number of software vendors have released hardware-independent machine-vision software in response both to the increased availability of direct-connect cameras and to the desire of some users to design vision systems that more closely match their specific needs. Peter Keppler, Common Vision Blox product manager for Stemmer Imaging, explained that although easy-to-use smart cameras accelerated the use of machine vision on production lines, many industrial customers now need the processing power and the flexibility of PCs. "Users are also aware of the advantages of dedicated tool sets that focus on their needs and assure a machine-vision application that can provide quick, reliable, accurate inspection," he said. "Because these users seek a cost-effective and flexible solution, hardware-independent third-party tools are the logical instrument."

When considering what type of machine-vision software to purchase, the main hardware to consider, aside from the camera itself, is capture hardware, said Pierantonio Boriero, product line manager for Matrox Imaging. But with the advent of open interface standards such as GigE Vision and IEEE 1394, a specialized acquisition device such as a frame grabber—and its hardware-specific software—is no longer needed. "Hardware independence means developers can work with any camera from any vendor as long as it conforms to the standard," he said. Now, developers must decide whether to develop software from the ground up or rely on third-party software tools to perform image capture, processing, and analysis.

One reason for developers' increased interest in writing their own machine-vision applications is the broad range of cameras available today, said Marilyn Matz, senior VP of vision software for Cognex, which unbundled its VisionPro acquisition software from its hardware last January. "Many models, sizes, interfaces, form factors, and technologies are available for a wide variety of prices, and customers want the flexibility to be able to choose the cameras that meet their specific application's needs," she said. "In addition, as the machine-vision industry has matured, so has the breadth of applications customers want to do."

The MIL software can process image data from a flexible printed-circuit panel. Courtesy of Matrox Imaging.

Many software vendors offer a hardware-independent package that combines a library for experienced programmers with a menu-driven, drag-and-drop GUI for users with less programming experience. "With a programming library such as MIL [Matrox Imaging Library], developers can add custom operators to an application, or they can use the library as building blocks," said Boriero. "Libraries give developers maximum flexibility. With menu-driven software, you're less likely to be able to extend the capabilities of the toolkit."

Some vendors also provide solution-specific tools, such as a package

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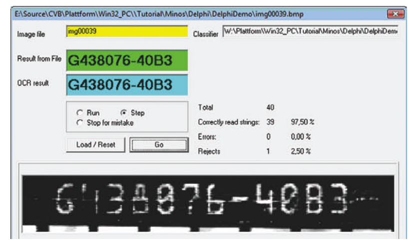
that only inspects BGAs (ball-grid arrays) or one dedicated to wafer surface inspection. Stemmer's Common Vision Blox supports the programmer with several optional tools but also gives free access to pure image data for the experts, said Keppler. It lets programmers stay with their pre-



In this optical character recognition application, the Minos tool of Common Vision Blox reads serial numbers on wafers. Courtesy of Stemmer Imaging.

ferred programming languages without losing any performance.

For many single-camera applications, a smart camera is preferable, but in most multi-camera situations, a PC-based vision system and its accompanying software package are more cost-effective than several smart cameras, said Matz. She explained that PC-based machine-vision software packages are preferable when an application requires the fastest performance as well as high resolution and a lot of flexibility. "PC processors are always going to be faster than smart camera processors," she said. "When you need the fastest performance with multicore CPUs or multiprocessors, you'll get the maximum horsepower from a PC. But there's a place for both of these approaches."

Most major machine-vision software packages include support for 32-bit and 64-bit processors, multicore CPUs and multiprocessor PCs, and both 2-D and 3-D calibration, as well as Windows and Linux operating systems. Support for 64-bit processors is becoming increasingly important as more customers want higher resolution to find smaller defects, as well as the ability to do flat-panel display and whole-wafer inspection, said Matz. □

JIM IULIANO
President and CEO
Azimuth Systems
Acton, MA

Jim Iuliano has more than a decade of CEO experience in the semiconductor, life sciences, display, and optical systems industries. Prior to joining Azimuth Systems, he was an entrepreneur in residence at North Bridge Venture Partners. Previously, he served as president and CEO of E Ink, a privately held materials technology company, and before that he headed Molecular Devices, an analytical instrumentation company in life sciences. Earlier in his career, Iuliano worked at both IBM and VLSI Technology. He holds a BS from Boston College and an MBA from Harvard Business School.

Contributing editor Larry Maloney conducted a phone interview with Iuliano on the need for innovative test solutions for sophisticated communications devices.

Complexity breeds quality challenges

Q: How will the economic slump affect the wireless industry?

A: Certainly the economic slowdown will have an impact. Among communications companies, there will be some downward revisions in revenue and growth estimates, as well as tightened capital expansion budgets. Still, the underlying trend toward growth in wireless technology remains healthy, with increasing mobile access to more and more multimedia applications. We see projections that, within five years, mobile devices will actually eclipse PC connections.

Q. What is Azimuth's niche in wireless communications test?

A: Our core technology is testing the impact that mobility has on sending and receiving IP (Internet protocol) packets. For example, how will my device perform as it is roaming, and what's the impact of mobility on data-transmission integrity? So, we play at the nexus between quality of service and motion.

Our main value add is that we conduct all our tests in a controlled environment, as opposed to traditional open-air tests where a device is constantly assaulted by innumerable outside RF interferences. Our controlled environment allows us to test performance metrics one at a time for superior quality in RF testing. We've also built our test systems from the ground up to handle sophisticated communications technology, such as MIMO (multiple-input, multiple-output) and OFDM (orthogonal frequency-division multiplexing). Finally, our products are scalable, easy to configure, and readily integrated with other tools in test labs.

Q: What special test challenges result from the proliferation of new communications technologies?

A: A good example is the convergence of WiFi, which started as a data-communications technology, with voice-based cellular. Our response at Azimuth is to develop a comprehensive suite of automated fixed-mobile convergence test solutions for issues such as call quality, dropped calls, and battery life. In this effort, we've taken our WiFi test experience and partnered with Agilent, which has long experience in cellular test. This will be a continuing strategy. As devices require more complicated testing, as in converged environments, we hope to partner with other companies to design integrated, turnkey test solutions for our customers.

Q: Which standard do you see dominating 4G technology?

A: There are multiple contenders, most notably WiMAX and LTE (long-term evolution). WiMAX plays very well in countries such as India that don't have an incumbent wired investment. LTE, on the other hand, has greater strength in areas that do have existing wired infrastructure. So, most of the large cellular carriers, such as AT&T, Vodafone, and Verizon, have opted for LTE. Our test platforms support both standards, and we're equally at home with open or proprietary systems.

Q: What was Azimuth's most significant new product of 2008?

A: This year, we introduced in beta the ACE MX, which supports frequencies between 450 MHz and 6 GHz. It meets the needs of all relevant wireless technologies and standards in the world of cellular, including LTE. This new platform, which will be on the market in the first quarter of 2009, delivers excellent RF fidelity and ease of use. And it's scalable, covering applications from entry-level solutions up to the most sophisticated research needs. We believe that the MX will open up new markets for us and be our major growth driver in 2009 and beyond. T&MW

Jim Iuliano addresses more questions on technology convergence and test partnerships in the online version of this interview: www.tmworld.com/2008_12.

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